



RIGOL

USB 3.0 Signal

Compliance Analysis Test

User Guide

May.2025

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1 Document Overview

This manual describes how to use RigolCTS. RigolCTS software is intended to work with **RIGOL**'s DS80000 series digital oscilloscopes to perform USB 3.0 compliance analysis.

To properly use the software, read this manual before you begin.

Main Topics in this Manual

- Test Device Connection
- Software Installation and Application
- Introduction to the USB 3.0 Protocol

Format Conventions in this Manual

- The menu name on the software is indicated by the format of "Menu Name (Bold) + Character Shading" or enclosed with quotes.
- The next step of the operation is denoted by an arrow ">" in the manual.

2 Introduction to the USB 3.0 Protocol

USB (Universal Serial Bus) was created in 1995. Since then, it has evolved from the early USB1.0 Low Speed, USB1.1 Full Speed to the USB2.0 High Speed specification in 2000. In late 2008, the *USB 3.0 SuperSpeed Specification* was released. In 2019, the USB4 protocol was released, with data rate up to 40 Gbps.

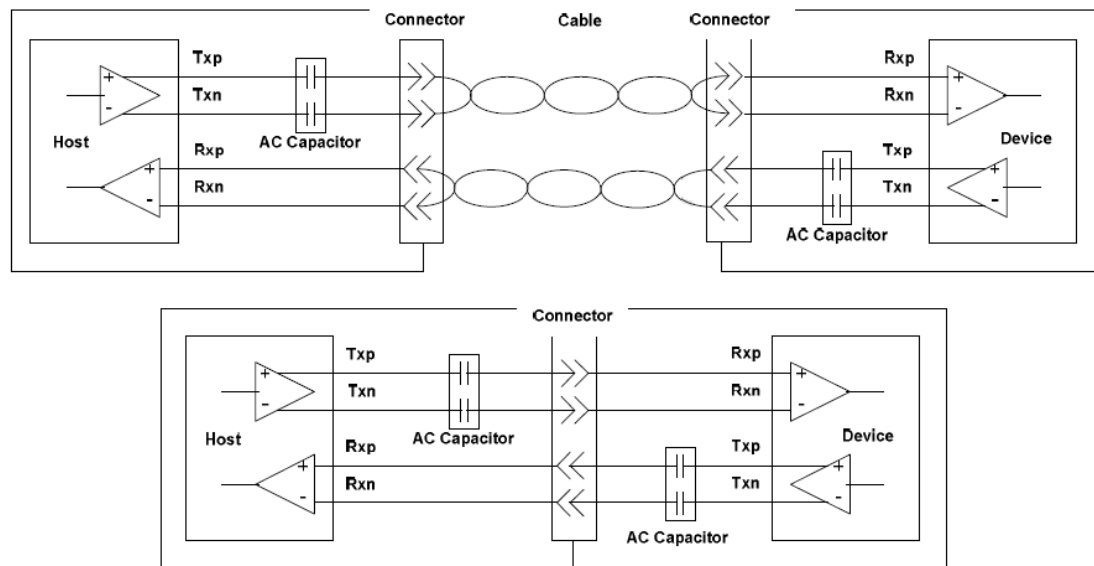
USB3 includes the following three generations of specifications:

Name	Original Name	Data Rate
USB 3.2 Gen1	USB 3.0	5 Gbps
USB 3.2 Gen 2	USB 3.1	10 Gbps
USB 3.2 Gen 2X2	USB 3.2 Gen1	20 Gbps (10 Gbps/lane, 2 lanes)

USB 3.2 Gen1 is widely used in STD-A/STD-B and Type-C interface for high-speed storage and transmission scenarios. This PC software is only available for the compliance test of USB 3.2 Gen1 SuperSpeed signal.

2.1 Product and Interface

The following figure shows the lane model of USB 3.0.



In the USB 3.0 Specification, differential signaling is used primarily, rather than the single-level pattern. Differential signal is transmitted through two cables. The voltage difference between the two cables shows its logic state. Therefore, this transmission mode features strong anti-interference capability.

- There are four types of USB 3.0 products: Device, Host, Hub upstream, and Hub downstream.
- The USB 3.0 interfaces includes four types: STD-A, STD-B, Micro AB, and Type-C.

2.2 Test Signal

The DUT signals required for the USB3.2 Gen1 Transmitter Compliance Test include LFPS (Low Frequency Periodic Signaling) and 5G signaling.

2.2.1 Low Frequency Periodic Signaling Test

The low frequency periodic signal (LFPS) is used for sideband communication between two ports across a link that is in a low-power link state. This signal is also used when a link is under training, or when a downstream port issues Warm Reset to reset the link.

LFPS signals include:

- **Polling.LFPS:** It is one of the sub-states of Polling. If device connection or link state changes, the LFPS signal is sent to detect device and make negotiations across the link partner.
- **Ping.LFPS:** indicates the regular detection of connectivity between devices in a low-power state, such as U1.
- **Warm Reset:** resets the link when there is a link problem or a reconfiguration is required.
- **U1/U2:** notifies the device to exit from the U1 and U2 state and returns to normal state.
- **U3 Wakeup:** indicates that the device wakes up during its suspended state when it receives an external wakeup signal (such as trigger action, a wakeup command sent from another device).

This section describes how to perform the compliance test for the Polling.LFPS signal. The Polling.LFPS signal is a Square waveform (with duty cycle close to 50%, 20 to 100 ns cycles, 10 to 50 MHz), with each burst lasting 1.0 μ s (with 32 cycles), as shown in *Figure 2.1*.

2.2.2 5G Signaling Test

When the DUT enters normal or high-speed data transmission mode, it begins to send 5 Gbps high-speed data. The USB 3.2 Gen1 test signal has 9 compliance patterns (CP0 through CP8). The transmitter compliance test needs to acquire CP0 and CP1, with which you can perform tests on the transmitter from different dimensions to ensure that its performance meets the requirements of USB 3.2 Gen 1.

- **CP0:** indicates a pseudo-random data pattern using 8b/10b encoding to simulate the real data transmission scenarios. It can be used in eye diagram, total jitter test, etc.
- **CP1:** D10.2, a continuous alternating 01 pattern, equivalent to the clock signal of 2.5 GHz frequency.

It is mainly used to calibrate instrument errors and separate jitter components, to provide reference clock for the test. It can also be used for spread spectrum clocking (SSC) and random jitter (RJ) testing.

2.3 Compliance Test

Perform the LFPS test, 5G signaling test (5G transmitter SSC test, 5G transmitter eye short channel test, and 5G transmitter eye far end test) according to Specifications.

2.3.1 LFPS Compliance Test

The following figure shows the waveform of the Polling.LFPS signal.

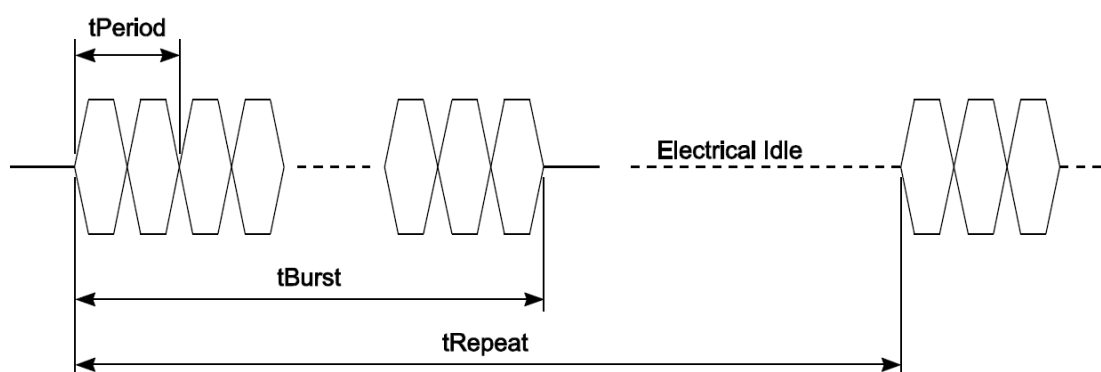


Figure 2.1 Polling.LFPS Signal Waveform

- **LFPS Burst:** indicates the transmission of continuous LFPS signal over a period of time defined by t_{Burst} .

- LFPS Sequence: indicates the transmission of a single LFPS burst of duration t_{Burst} over a period of time defined by t_{Repeat} .
- t_{Period} : indicates the period of an LFPS cycle.
- Electrical Idle: indicates the interval between two contiguous LFPS bursts.

The following parameters of the LFPS signal are tested according to specifications.

- LFPS Tburst Test
- LFPS Trepeat Test
- LFPS Tperiod Test
- LFPS Trisingedge Test
- LFPS Tfallingedge Test
- LFPS Tduty cycle Test
- LFPS AC Common Mode Voltage Test
- LFPS Peak-Peak Differential Voltage Test

Table 2.2 LFPS Signal Test Standard

Test Item	Test Parameter	Min.	Max.
LFPS Tburst Test	Tburst	0.6 μ s	1.4 μ s
LFPS Trepeat Test	Trepeat	6 μ s	14 μ s
LFPS Tperiod Test	Tperiod	20 ns	100 ns
LFPS Trisingedge Test	Trisingedge	-	4000 ps
LFPS Tfallingedge Test	Tfallingedge	-	4000 ps
LFPS Tduty cycle Test	Tduty cycle	40%	60%
LFPS AC Common Mode Voltage Test	AC Common Mode Voltage	-	100 mV
LFPS Peak-Peak Differential Voltage Test	Peak-to-Peak Differential Voltage	800 mV	1200 mV

2.3.2 SSC Compliance Test

Spread spectrum clocking is often used on the circuit of the main board of PC, aiming to reduce electromagnetic emissions (EMI). In USB 3.0, SSC modulation rate and SSC deviation are required to be tested.

SSC is closely related to the USB 3.0 chip-to-chip input clock. If the SSC of the input clock fails to comply with the requirements, then the SSC of the output signal of USB 3.0 will also fail to pass the test.

The 5G Transmitter SSC Test includes the following test items according to the Specification requirement.

- SSC Freq Dev Trough
- SSC Freq Dev Peak
- SSC Modulation
- SSC Slew Rate
- SSC df/dt

Table 2.3 5G Transmitter SSC Test Standard

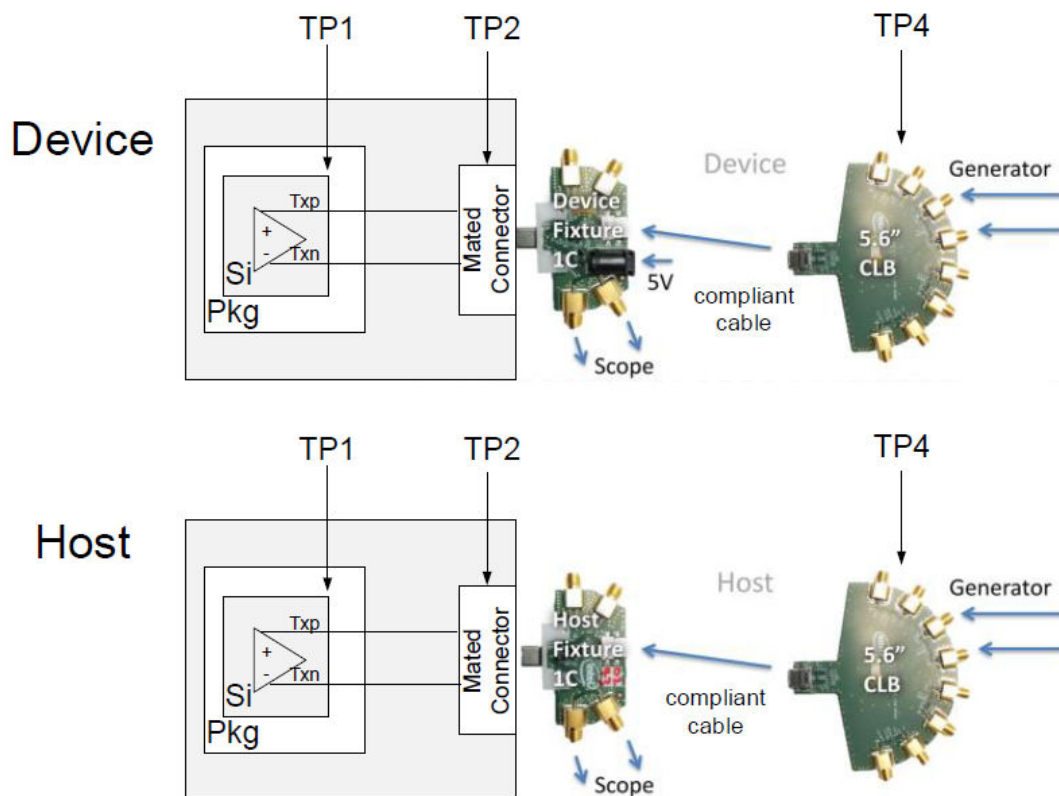
Test Item	Measurement Parameter	Min.	Max.
SSC Freq Dev Trough	Frequency deviation trough (ppm)	-5300.0 ppm	-3700.0 ppm
SSC Freq Dev Peak	Frequency deviation peak (ppm)	-300.0 ppm	300.0 ppm
SSC Modulation	Modulation frequency (kHz)	30 kHz	33 kHz
SSC df/dt	Frequency variation rate over time (ppm/μs)	-	1250 ppm/μs
SSC Slew Rate	SSC slew rate (ms)	-	10.0 ms

2.3.3 Eye Diagram Compliance Test

In the eye diagram and jitter tests, special test patterns are required.

- For the eye diagram test, CP0 (D0.0 scrambled) is required for deterministic jitter (Dj) measurement.
- For jitter test, CP0 or CP1 (D10.2) is required for random jitter (Rj) measurement.

The Specification defines the eye short channel (TP2) and eye far end test (TP4), as shown in the following figure.



Test Point	Description
TP1	Transmitter silicon pad
TP2	Transmitter port connector midpoint
TP4	Receiver silicon pad

According to the Specification, the eye compliance test consists of the following test items.

- 5G Transmitter Eye Short Channel Test
 - TP2 Short Channel Random Jitter
 - TP2 Short Channel Maximum Deterministic Jitter
 - TP2 Short Channel Total Jitter at BER-12 (total jitter of TP2 short channel at 10^{-12} BER)
 - TP2 Short Channel Template
 - TP2 Short Channel Differential Out Voltage

- 5G Transmitter Eye Far End Test
 - TP4 Long Channel Random Jitter
 - TP4 Long Channel Maximum Deterministic Jitter
 - TP4 Long Channel Total Jitter at BER-12 (total jitter of TP4 long channel at 10^{-12} BER)
 - TP4 Long Channel Template
 - TP4 Long Channel Differential Out Voltage

Table 2.5 5G Transmitter Eye Short Channel Test and Transmitter Eye Far End Test

Test Item	Measurement Parameter	Min.	Max.
5G Transmitter Eye Short Channel Test			
TP2 Short Channel Differential Out Voltage	Differential Output Voltage	100 mV	1200 mV
TP2 Short Channel Total Jitter at BER-12	Total Jitter (BER = $1e-12$)	-	132 ps
TP2 Short Channel Maximum Deterministic Jitter	Deterministic jitter	-	86 ps
TP2 Short Channel Random Jitter	Random Jitter	-	3.27 ps
TP2 Short Channel Template	Eye Mask Test	0.000 (fixed value)	0.000 (fixed value)
5G Transmitter Eye Far End Test			
TP4 Long Channel Differential Out Voltage	Differential Output Voltage	100 mV	1200 mV
TP4 Long Channel Total Jitter at BER-12	Total Jitter (BER = $1e-12$)	-	132 ps
TP4 Long Channel Maximum Deterministic Jitter	Deterministic Jitter	-	86 ps
TP4 Long Channel Random Jitter	Random Jitter	-	3.27 ps

Test Item	Measurement Parameter	Min.	Max.
TP4 Long Channel Template	Eye Mask Test	0.000 (fixed value)	0.000 (fixed value)

3 Test Device

Before performing the USB3.0 compliance test, you will need to obtain the required devices and software, and calibrate the oscilloscope.

Table 3.1 Devices Required

Device	Description
Digital Oscilloscope	- Performance Specifications: Min. bandwidth: 13 GHz Min. sample rate: 40 GSa/s - Recommended Devices: RIGOL DS80000 series oscilloscope (with USB3.0 compliance analysis supported) (required to install the DS80000-USB3C option)
DUT	The Devices under Test (DUTs) include the following four types: - Device (typical DUT, e.g. Removable hard drive 500 GB, USB 3.0 supported) - Host (typical DUT, e.g. PC with USB 3.0 interface, use XHSETT tool to control the USB interface to send test signals.) - Hub Upstream, (typical DUT, e.g. USB3 Hub) - Hub Downstream, (typical DUT, e.g. USB3 Hub)
Test Fixture	- DEVICE FIXTURE 1C - HOST FIXTURE 1C - COMPLIANCE LOAD BOARD - Fixture power cable
Cable	- Type-C cable x1 - SMA(M)-SMA(M) cable x2, with equal length; SMA(F)-SMA(F) adapter x2 - SMA(M)-SMA(M) cable x1

Table 3.2 Digital Oscilloscope and DUT



DS80000 Series Digital Oscilloscope

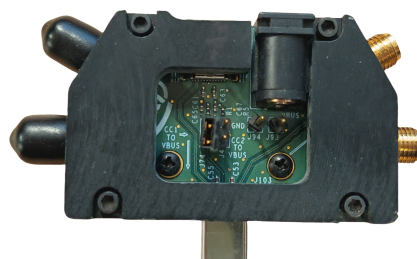


500 GB Removable Hard Drive

Table 3.3 Fixture



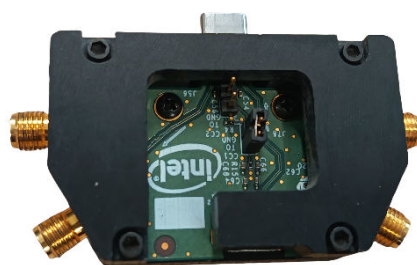
DEVICE FIXTURE 1C (Front)



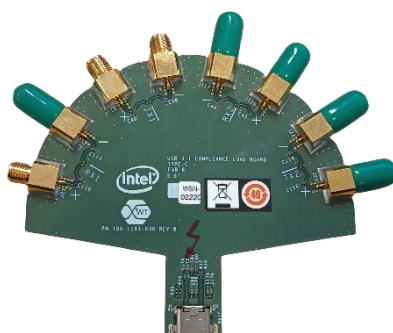
DEVICE FIXTURE 1C (Back)



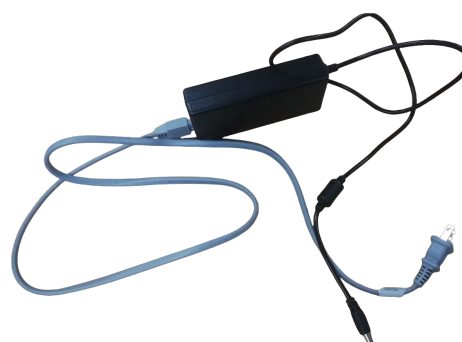
HOST FIXTURE 1C (Front)



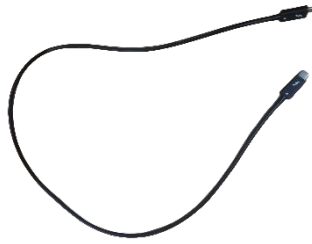
HOST FIXTURE 1C (Back)



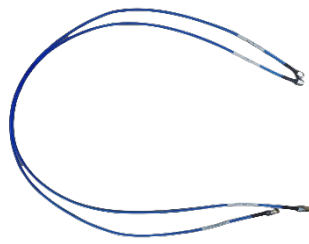
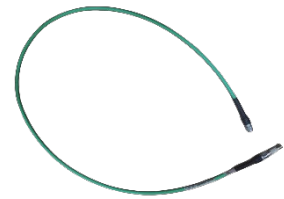
COMPLIANCE LOAD BOARD



Fixture power cable

Table 3.4 Cable

Type-C cable

SMA(M)-SMA(M) cable,
SMA(F)-SMA(F) adapter

SMA(M)-SMA(M) cable

4 DUT Test

There are four types of Devices under Test (DUTs). For different tests, use different types of DUTs.

- **Device**
Used to test the physical layer signal quality of USB 3.0 devices such as USB storage device, removable hard drive, camera, etc.
- **Host**
Used to test the USB 3.0 port performance of a host (e.g. computer, server) to ensure that the host can communicate properly with externally connected devices. For the Host test, the DUT is required to actively send out LFPS, CP0, and CP1 patterns.
- **Hub Upstream**
Used to test the USB3.0 hub's upstream port performance to ensure that the hub can communicate properly with the host.
- **Hub Downstream**
Used to test the USB 3.0 hub's downstream port performance to ensure that the hub can communicate properly with externally connected devices.

The USB 3.0 connection types are as follows:

- **Type-C**
Suitable for devices with USB 3.0 Type-C interface, available for physical layer compliance test of USB 3.0 (5Gbps) and higher (e.g. USB3.1 Gen1/Gen2, USB4).
- **STD A to STD B**
Used for the physical layer compliance test for devices with USB 3.0 Type-A (Host) and Type-B (Device) interfaces.
- **STD A to Micro B**
Used for the physical layer compliance test for devices with USB 3.0 Micro B interface.
- **Tethered**
Available for various interface types of USB 3.0 cables, including Type-A to Type-B, Type-A to Micro B, Type-C to Type-C, and etc. It is suitable for physical layer compliance test of cables across the devices under data transfer.
- **CAPTIVE Device**
Suitable for testing USB 3.0 devices with built-in cables (i.e. cables not detachable), such as some USB key, dongle, etc. CAPTIVE Device fixture enables you to properly connect the built-in cables with test instruments based on the

characteristics of this type of device, and complete the physical layer compliance test for the device.



TIP

Tethered is not available for the Host test and the Hub Downstream test.

4.1 Device Test

This section takes Type-C interface fixture as an example to introduce the connection methods for the Device test.

Test Device Required

- **Oscilloscope:** DS81304
- **DUT:** 500 GB removable hard drive with USB Type-C interface.
- **Fixture:** DEVICE FIXTURE 1C (hereinafter abbreviated as Device 1C), COMPLIANCE LOAD BOARD, fixture power cable
- **Cable:** Type-C cable, two SMA(M)-SMA(M) cables+two SMA(F)-SMA(F) adapters (or two SMA(M)-SMA(F) cables), one SMA(M)-SMA(M) cable

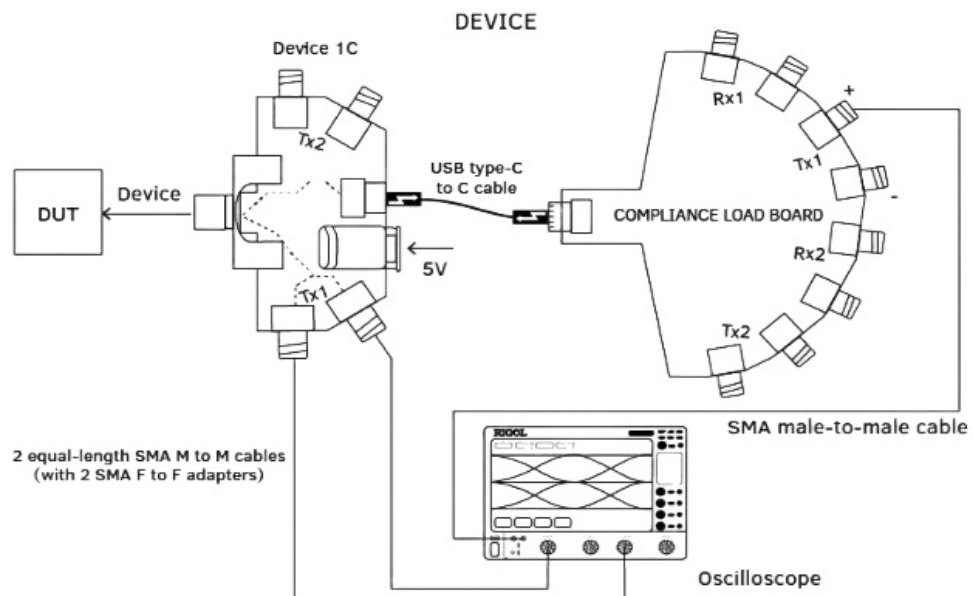
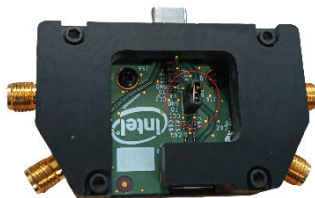


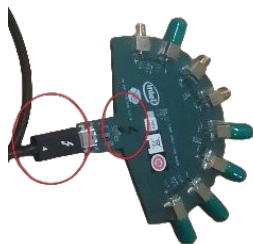
Figure 4.1 Connection Diagram of Device Type-C Fixture

Connection Procedures:

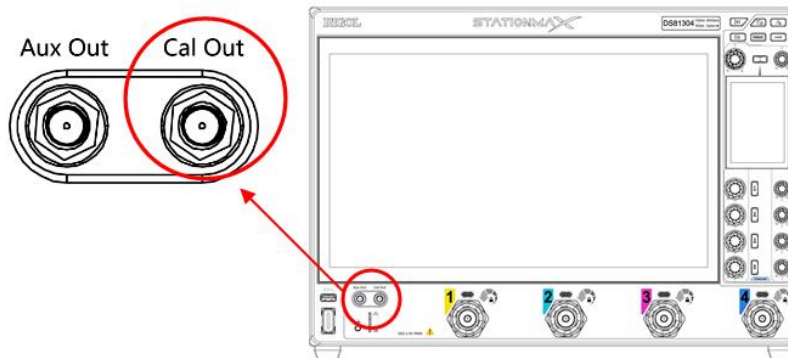
1. Connect the USB Type-C interface of the test device (removable hard disk) to the device test fixture (Device 1C).
2. Provide 5V VBUS power source to the fixture. (Note that short-circuit the jumper cap of the fixture properly, as shown in the red circle indicated below.)



3. Connect the COMPLIANCE LOAD BOARD to the test fixture (Device 1C) by using one 1-meter Type-C to Type-C cable. (Pay attention to the cable connection direction. When connecting to the fixture with the cable, note that the USB icon on one end of the cable should be faced upward, as indicated in the red circle below.)



4. Connect the Tx1+ connector of the test fixture (COMPLIANCE LOAD BOARD) to the CAL OUT output connector of DS81304 by using one SMA(M)-SMA(M) cable, as shown in the figure below.



5. Connect the Tx1+ and Tx1- interfaces of the test fixture (Device 1C) to CH1 and CH3 (or CH2 and CH4) of the oscilloscope respectively by using two SMA(M)-

SMA(F) cables. You can also use the two equal-length SMA(M)-SMA(M) cables to work with 2 SMA(F)-SMA(F) adapters to achieve it.

4.2 Host Test

The following section takes Type-C interface fixture as an example to introduce the connection methods for the host test.

Test Device Required

- **Oscilloscope:** DS81304
- **DUT:** Desktop PC with USB Type-C interface
- **Fixture:** HOST FIXTURE 1C (hereinafter abbreviated as Host 1C), COMPLIANCE LOAD BOARD, fixture power cable
- **Cable:** Type-C cable, two SMA(M)-SMA(M) cables+two SMA(F)-SMA(F) adapters (or two SMA(M)-SMA(F) cables), one SMA(M)-SMA(M) cable

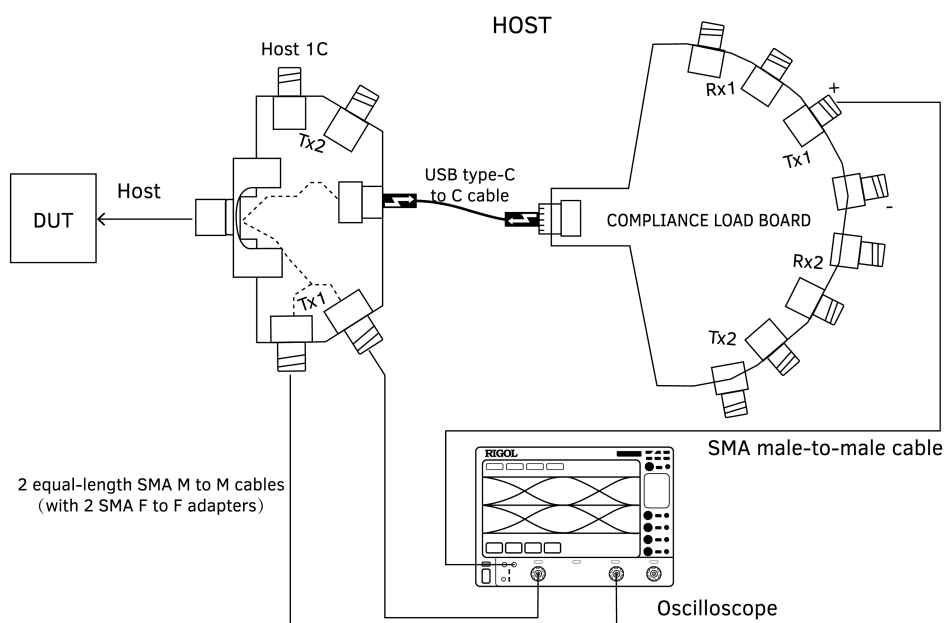


Figure 4.2 Connection Diagram of Host Type-C Fixture

TIP

When starting to perform the Host test, the USB interfaces of the current host may fail to work, and all the other external devices may fail to work with the USB interface to operate the software, making you unable to operate the software with the USB-connected mouse. You can use the virtual desktop to use the XHSETT tool to control the USB interface of the host (take

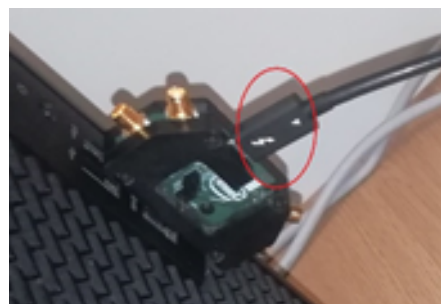
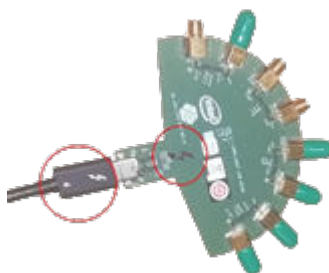
USB Type-C of the desktop PC as an example) to enter the compliance test mode to send the signal to be tested. As for how to use the XHSETT tool, refer to descriptions in *XHSETT Tool*.

Connection Procedures:

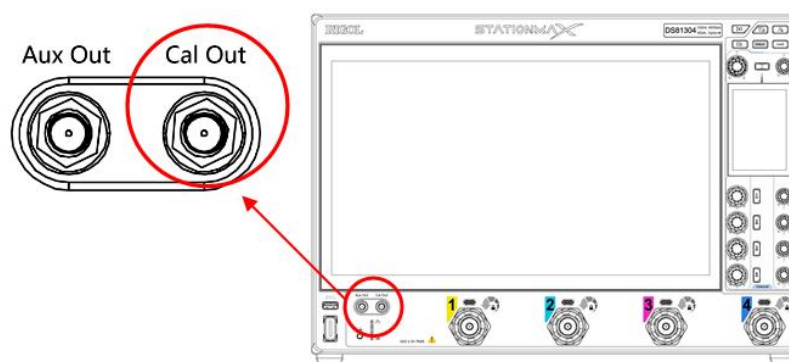
1. Connect the Type-C interface of the DUT (desktop PC) to the test fixture (Host 1C). Note that short-circuit the jumper cap of the fixture properly, as shown in the red circle indicated below.



2. Connect the COMPLIANCE LOAD BOARD to the test fixture (Host 1C) by using one 1-meter Type-C to Type-C cable. (Pay attention to the cable connection direction. When connecting to the fixture with the cable, note that the USB icon on one end of the cable should be faced upward, as indicated in the red circle below.)



3. Connect the Tx1+ connector of the test fixture (COMPLIANCE LOAD BOARD) to the CAL OUT output connector of DS81304 by using one SMA(M)-SMA(M) cable, as shown in the figure below.



4. Connect the Tx1+ and Tx1- interfaces of the test fixture (Host 1C) to CH1 and CH3 (or CH2 and CH4) of the oscilloscope respectively by using two SMA(M)-SMA(F)

cables. You can also use the two equal-length SMA(M)-SMA(M) cables to work with two SMA(F)-SMA(F) adapters to achieve it.

4.3 Hub Upstream Test

The following section takes Type-C interface fixture as an example to introduce the connection methods for the hub upstream test.

Test Device Required

- **Oscilloscope:** RIGOL DS81304
- **DUT:** USB Hub. Connect the USB Hub's downstream port to the USB Type-C interface of the removable hard drive.
- **Fixture:** DEVICE FIXTURE 1C (hereinafter abbreviated as Device 1C), COMPLIANCE LOAD BOARD, fixture power cable
- **Cable:** Type-C cable, two SMA(M)-SMA(M) cables+two SMA(F)-SMA(F) adapters (or two SMA(M)-SMA(F) cables), one SMA(M)-SMA(M) cable

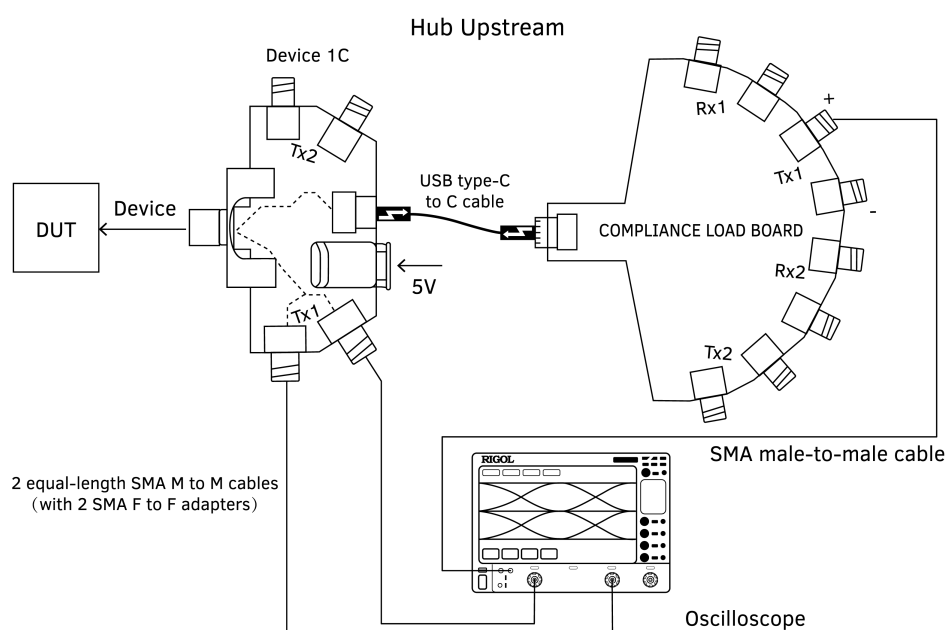


Figure 4.3 Connection Diagram of Hub Upstream Type-C Fixture

Connection Procedures:

- Connect the USB hub upstream port of the test device to the device test fixture (Device 1C). Provide 5V VBUS to the fixture (Device 1C).

- Connect the COMPLIANCE LOAD BOARD to the test fixture (Device 1C) by using a 1-meter Type-C to Type-C cable.
- Connect the Tx1+ connector of the test fixture (COMPLIANCE LOAD BOARD) to the CAL OUT output connector of DS81304 by using one SMA(M)-SMA(M) cable.
- Connect the Tx1+ and Tx1- interfaces of the test fixture (Device 1C) to CH1 and CH3 (or CH2 and CH4) of the oscilloscope respectively by using two SMA(M)-SMA(F) cables. You can also use the two equal-length SMA(M)-SMA(M) cables to work with 2 SMA(F)-SMA(F) adapters to achieve it.

4.4 Hub Downstream Test

The following section takes Type-C interface fixture as an example to introduce the connection methods for the hub downstream test.

Test Device Required

- **Oscilloscope:** RIGOL DS81304
- **DUT:** USB Hub. Connect the USB Hub's upstream port to the USB Type-C interface of the PC.
- **Fixture:** HOST FIXTURE 1C (hereinafter abbreviated as Host 1C), COMPLIANCE LOAD BOARD, fixture power cable
- **Cable:** Type-C cable, two SMA(M)-SMA(M) cables+two SMA(F)-SMA(F) adapters (or two SMA(M)-SMA(F) cables), one SMA(M)-SMA(M) cable

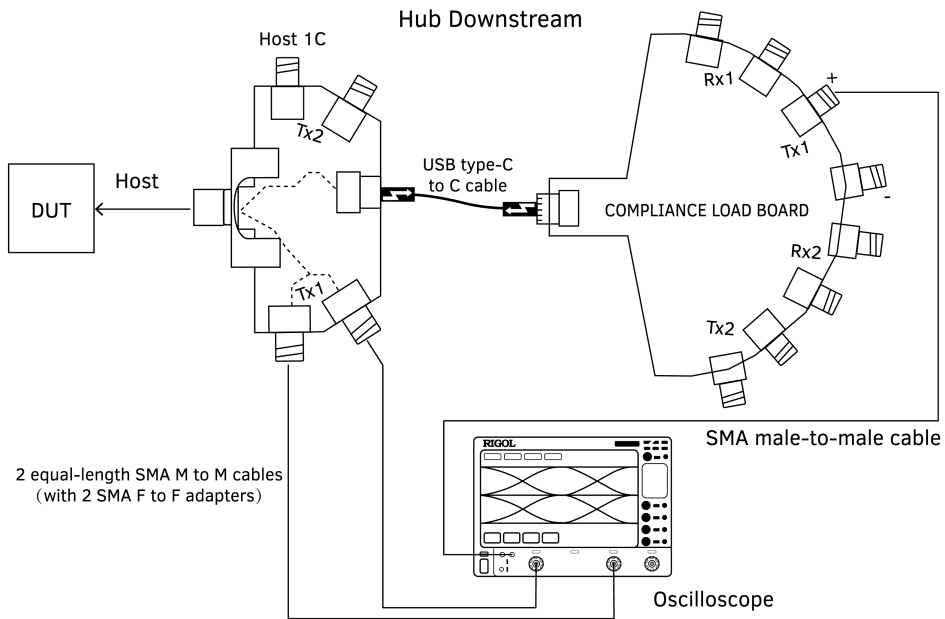


Figure 4.4 Connection Diagram of Hub Downstream Type-C Fixture



TIP

When performing the Hub Downstream test, use the XHSETT tool to control the USB3 host USB interface to enter the compliance test mode to send the signal to be tested. As for how to use the XHSETT tool, refer to descriptions in *XHSETT Tool*.

Connection Procedures:

1. Connect the USB Hub downstream port of the DUT to the test fixture (Host 1C).
2. Connect the COMPLIANCE LOAD BOARD to the test fixture (Host 1C) by using one 1-meter Type-C to Type-C cable.
3. Connect the Tx1+ connector of the test fixture (COMPLIANCE LOAD BOARD) to the CAL OUT output connector of DS81304 by using one SMA(M)-SMA(M) cable.
4. Connect the Tx1+ and Tx1- interfaces of the test fixture (Host 1C) to CH1 and CH3 (or CH2 and CH4) of the oscilloscope respectively by using two SMA(M)-SMA(F) cables. You can also use the two equal-length SMA(M)-SMA(M) cables to work with 2 SMA(F)-SMA(F) adapters to achieve it.

5 Software Installation and Application

RigolCTS software is intended for remote control of **RIGOL**'s DS80000 series digital oscilloscopes to perform USB 3.0 compliance analysis.

5.1 To Install and Run the Software

The installation program for the USB 3.0 compliance test is RigolCTS-Setup.exe.

Double-click the installation program to install the program. After installation is completed, a shortcut icon of the program appears on the PC desktop. If you launch the software for the first time, you need to run it as administrator. Right-click on the



icon **RigolCTS**, and select "Run as Administrator" to launch the RigolCTS software. For the next launch, you just need to double-click on the shortcut icon enter the software interface.

Also, in the Windows system, you can click **Start** > **RIGOL** > **RigolCTS** to enter the software interface.

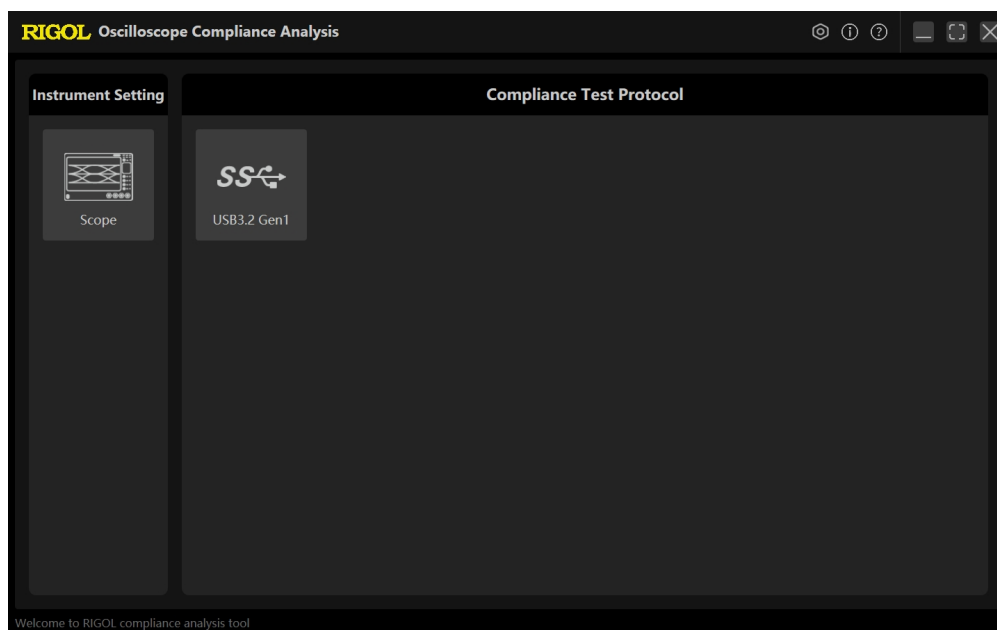


Figure 5.1 RigolCTS Main Interface

- Click on the icon  at the upper-right corner of the interface to set the software language. Currently, only Chinese and English are supported.

- To get any help information, click on the icon  at the upper-right corner of the interface to open the help document for the software.
- To obtain the software version, click on the icon  at the upper-right corner of the interface.

5.2 To Connect the Oscilloscope

1. Click on the Scope icon shown in *Figure 5.1* to enter the Scope Setup interface.
2. Input the IP address of the oscilloscope into the input field of "IP Address". Then click **Get Instrument Info** to connect the specified oscilloscope. If connected successfully, its basic information is displayed below.
3. Once the oscilloscope has been connected, you can remotely operate the oscilloscope with the software system for USB 3.0 compliance analysis test.
4. Click the Back icon at the upper-left corner of the interface to go back to the main interface of the software.

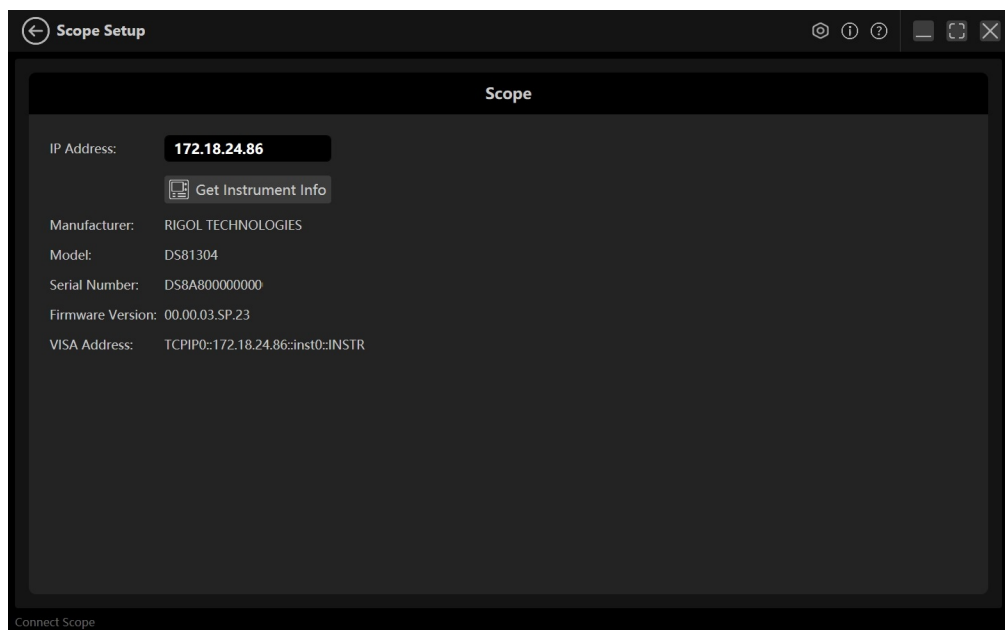


Figure 5.2 Oscilloscope Setup Interface

5.3 To Add a Test Project

Before starting the test, add a test project first. The procedures are as follows:

1. Click on the **USB 3.2 Gen1** icon to enter the USB 3.2 Gen1 project list interface.

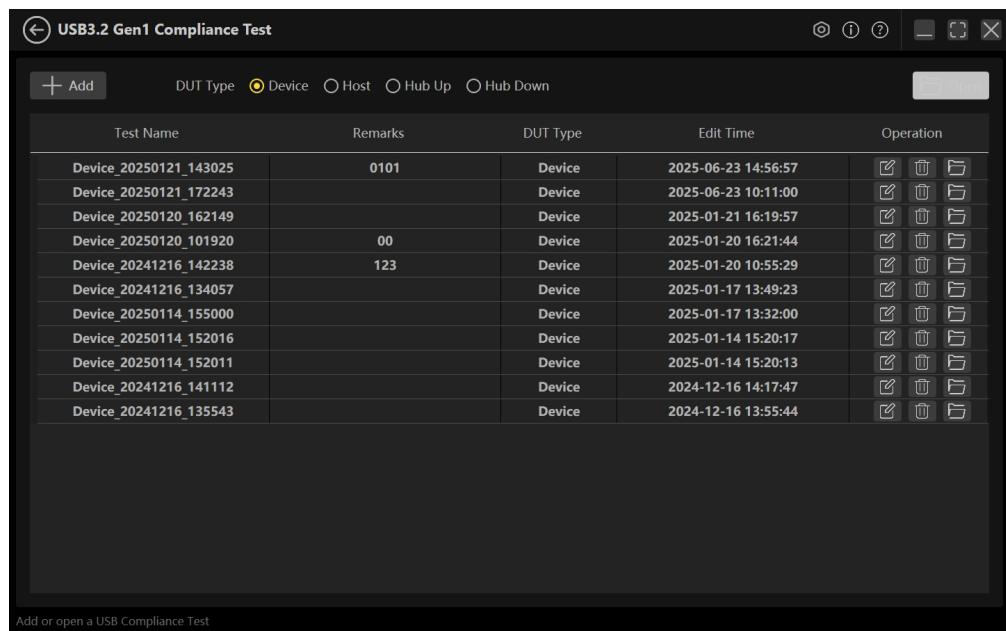


Figure 5.3 Project List Interface

2. Click **Add** to enter the menu below to configure the test project.

Add USB Compliance Analysis Session

Test Name: **Device_20250623_163825**

Remarks: **Please enter test remarks**

Edit Time: **2025-06-23 16:38:25**

DUT Type: ☒ Device ☐ Host ☐ Hub Up ☐ Hub Down

Add

3. Fill in the project information. The input fields of "Test Name" and "Edit Time" are filled in with default settings. The input field of "Remarks" can be left empty if no remarks is needed.

Select the DUT type. There are four options available. For details, refer to [DUT Test](#).

- Device
- Host
- Hub Upstream
- Hub Downstream

4. Click **Add** to add one project.



NOTE

When performing the Host test or Hub Downstream test, use the XHSETT tool to control the USB3 host and hub to enter the compliance test mode to send the signal to be tested. As for how to use the XHSETT tool, refer to descriptions in *XHSETT Tool*.

5.4 To Operate on the Project

In the "USB 3.2 Gen1 Compliance Test" interface, select the DUT type, and all the test projects of this DUT type are displayed.

To operate on the project, select the specified operation action under the "Operation" column of the project list. The operation actions include:

- Edit the project information
- Delete the test project
- Open the test project

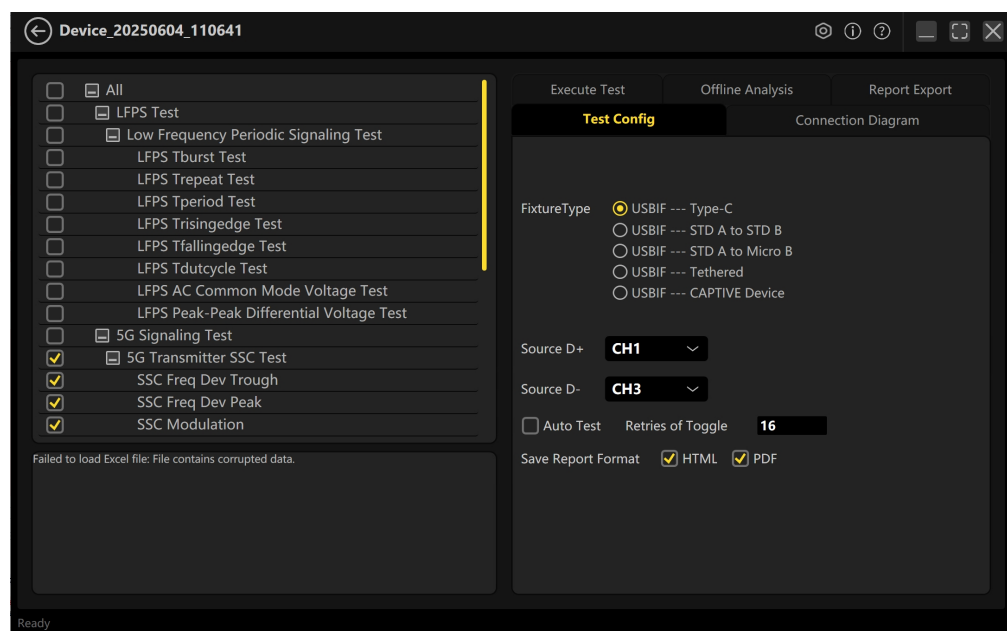


Figure 5.4 Test Project Operation Interface

5.5 To Select the Test Item

As shown in *Figure 5.4*, All the tests that need to be performed are displayed at the left side of the interface. You can check the checkbox of the specified test item to select the test item.

For the compliance test items and test pass specification supported by this compliance analysis solution, refer to *Compliance Test*.

View Test Item Details

Click the specified test item, and the details of the test item are displayed at the bottom-left part of the current interface. The information includes:

- Test
- Pass Limits
- Limit Set: USB 3.2 Specification version 1.1
- Margin Formula

Perform Multiple Tests at a Time

If all the tests are selected, the DUT sends the test signals in the following order.

1. Configures the DUT to send the LFPS signal.
2. Configure the DUT to send 5G CP0 signal.
3. Configure the DUT to send 5G CP1 signal.

In *To Execute the Test*, after all test signals are saved in sequence, the compliance analysis test for these signals is completed and a report is generated.

5.6 To Configure the Test

Click the "Test Config" tab at the right side of the interface to configure the following parameters.

Select the Fixture Type

The following types of USB interfaces are supported for the test. For details, please refer to *DUT Test*.

- Type-C
- STD A to STD B
- STD A to Micro B
- Tethered
- CAPTIVE Device

Configure the Source

Select the desired channel from the drop-down button of "Source D+" and "Source D-" according to the oscilloscope channel connected in the actual test.

Perform Auto Test

If you need to complete multiple test items at a time, check the checkbox of "Auto Test".

- For LFPS Test, Auto test is not supported as you need to disconnect the fixture from the DUT during the test.
- For 5G Signaling Test, "Auto Test" is supported. Once you check the checkbox of "Auto Test", the software will perform auto test for different test items. It will switch DUT pattern automatically based on different test items, configure the oscilloscope to capture the waveforms of the DUT, and perform USB 3.0 compliance analysis.

Auto Retries of Pattern Toggle

Pattern here specifically refers to CP0 and CP1 in USB 3.0 data transmission.

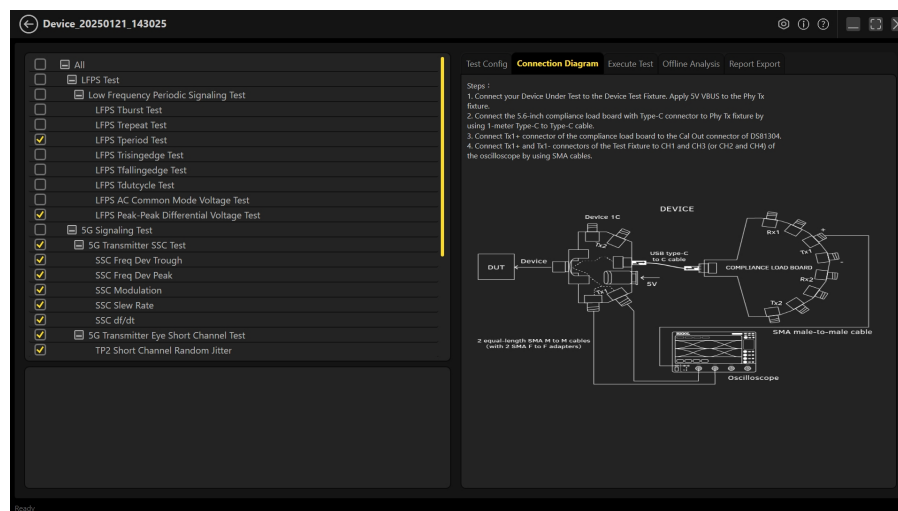
During the test, the software system will compare the received pattern with the standard pattern of CP0 and CP1 to see if the received pattern is compliant. If not compliant, the system automatically retries to toggle the pattern until the pattern received is compliant. After several retries of pattern toggle, the accuracy and stability of the data transmitted by the DUT can be assured, reducing the impact of probability of occurrence on the test results.

Report Format

The test report is saved to the oscilloscope as a "*.PDF" or "*.html" file.

5.7 Connection Diagram

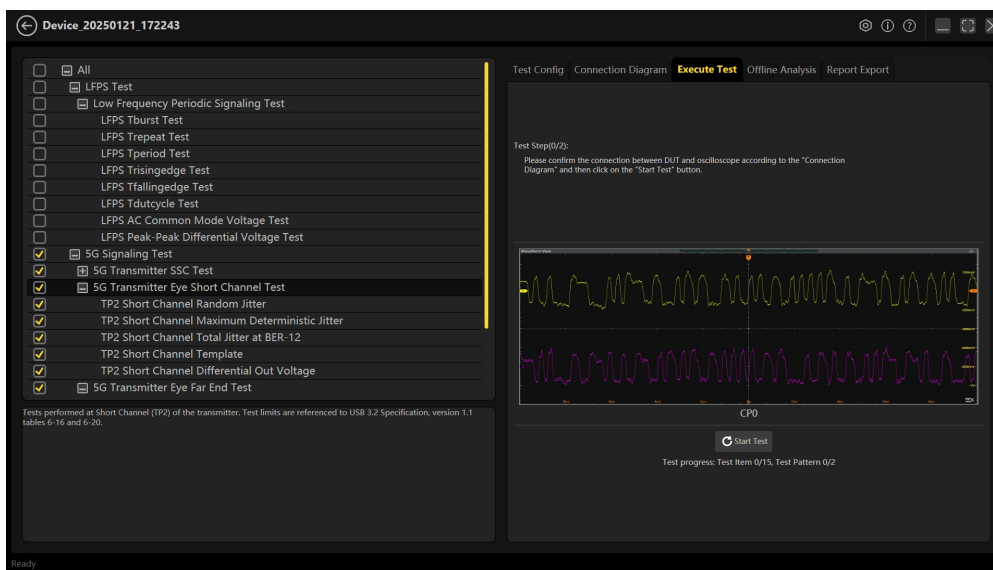
Click the **Connection Diagram** tab to enter the interface. Then you can connect the DUT device according to the test connection diagram and the steps, as shown in the figure below.



For the connection diagram of different DUT types and test fixtures, refer to descriptions in *DUT Test*.

5.8 To Execute the Test

Click the **Execute Test** tab to enter the test interface, then perform the test according to the test steps, as shown in the figure below.



1. First connect the devices properly according to the connection diagram shown in *Connection Diagram*.
2. Click **Start Test** to start the test.

5.8.1 LFPS Test

If you check the checkbox of **LFPS Test** at the left side of the screen, click the **Execute Test** tab, then click **Start Test** to start the test. The following figure is displayed.

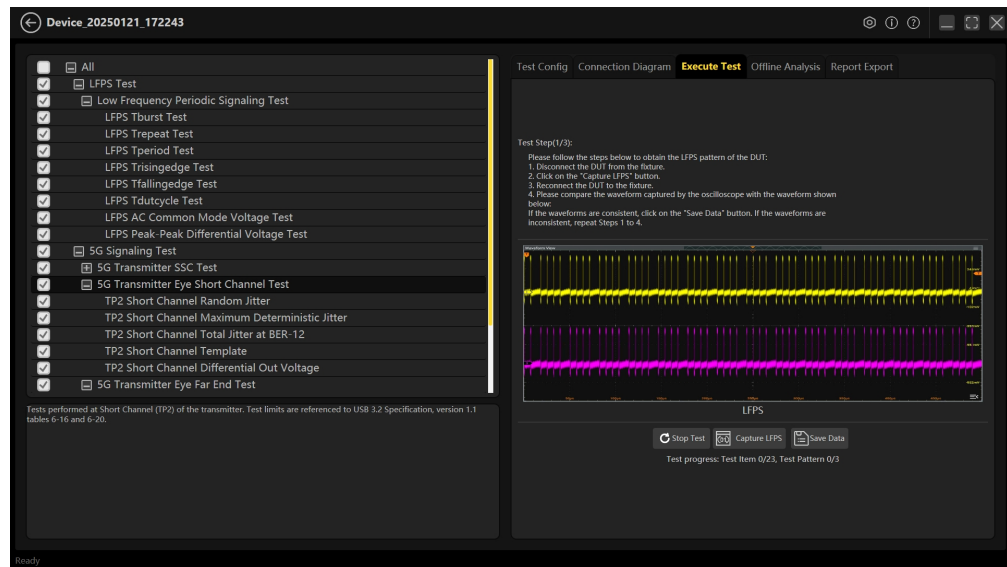


Figure 5.5 Execute Test Interface

Follow the "Test Step" to perform the test.

1. Disconnect the DUT from the fixture.
2. Click **Capture LFPS** to capture the LFPS test waveform sent by the DUT, as shown below.

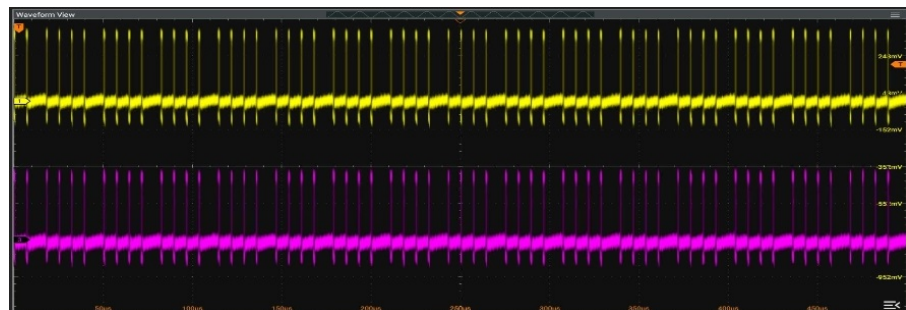
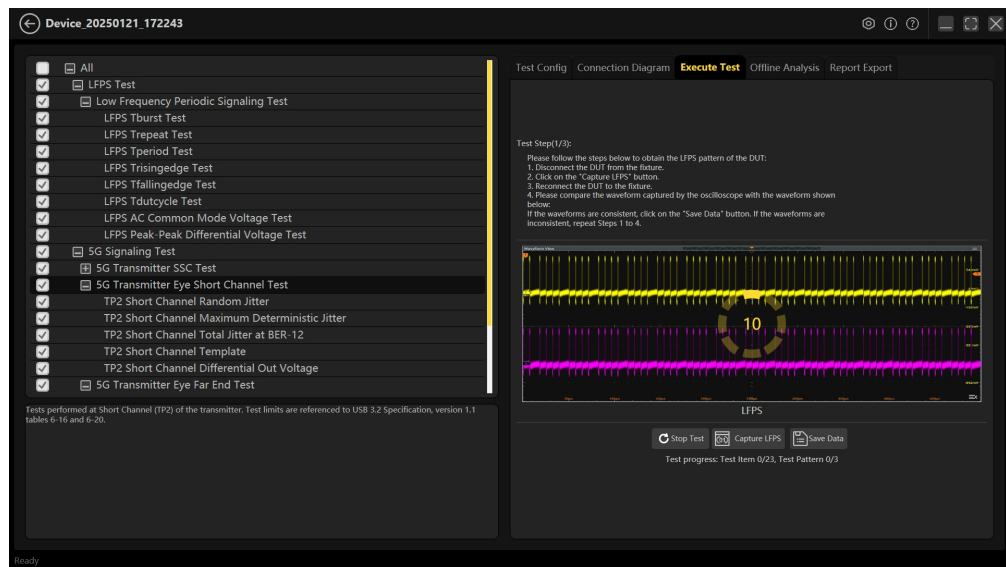


Figure 5.6 LFPS Waveform

3. Reconnect the DUT to the fixture.
4. Compare the waveform on the oscilloscope with the test waveform shown under the **Execute Test** tab. If they are consistent, click **Save Data** to save the waveforms.

After 30 s, the waveforms are saved as a file suffixed with "*.bin" and will be stored in the oscilloscope memory. You can access the saved LFPS waveform data file via FTP and move it to your PC. The data file complies with the USB3 Specification and can be used for future compliance test in *Offline Analysis*.



5. If the waveforms on the oscilloscope are not consistent with the test waveform shown under the **Execute Test** tab, repeat Step 1-4 to perform the test again.

After the test is completed, the test report for this test is displayed automatically.

During the test, you can stop the test any time by clicking **Stop Test**.

5.8.2 5G Transmitter Eye Short Channel Test and Transmitter Eye Far End Test

If you check the checkbox of **5G Transmitter Eye Short Channel Test** or **Transmitter Eye Far End Test** at the left side of the screen, click the **Execute Test** tab, then click **Start Test** to start the test. The following figure is displayed. During the test, you can stop the test any time by clicking **Stop Test**.

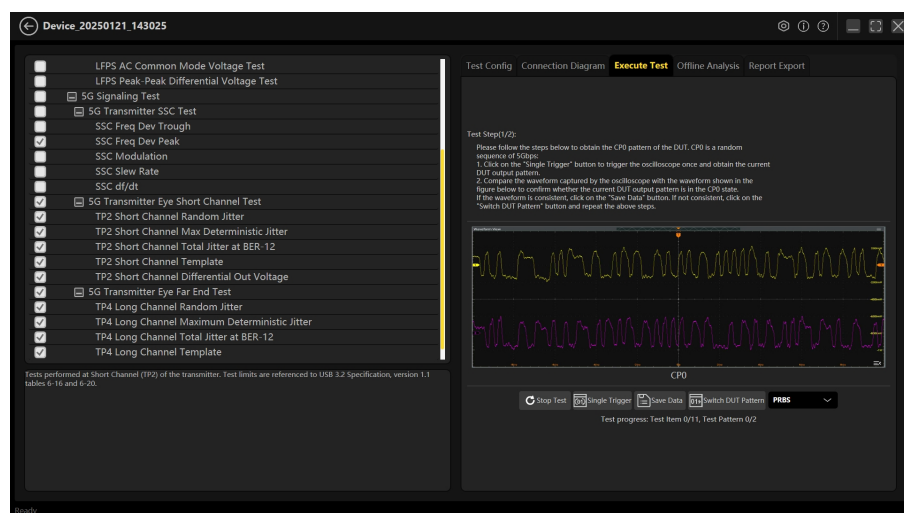


Figure 5.7 5G Transmitter Eye Short Channel Test and Transmitter Eye Far End Test

Follow the "Test Step" to perform the test. During the test, you can stop the test any time by clicking **Stop Test**.

For 5G Transmitter Eye Short Channel Test and Transmitter Eye Far End Test, the DUT is required to send the CP0 and CP1 pattern test signals.

The following section introduces how to capture CP0 and CP1 by manually configure the oscilloscope.



NOTE

If you enable **Auto Test**, CP0 and CP1 patterns are captured and tested automatically. You do not need to manually configure it to perform the test.

Capture CP0

Configure the oscilloscope to capture the CP0 pattern 5G test signal sent by the DUT. Then follow the "Test Step" to perform the test.

- Click **Single Trigger** to configure the oscilloscope to perform a single trigger on the CP0 pattern signal sent from the DUT.
- Compare the waveform on the oscilloscope with the test waveform shown under the **Execute Test** tab. You can view the waveform on the oscilloscope through the web control page.

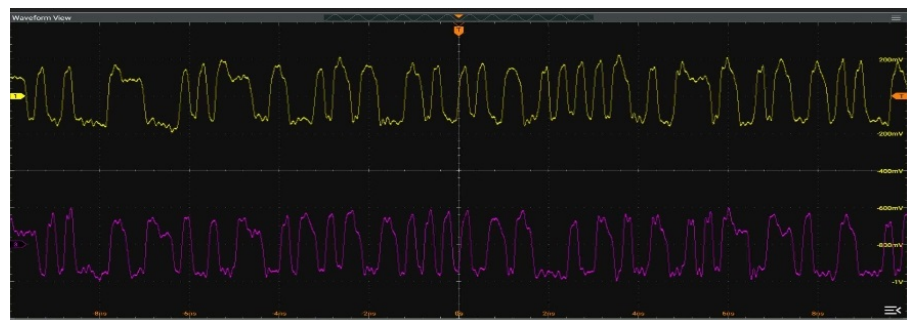
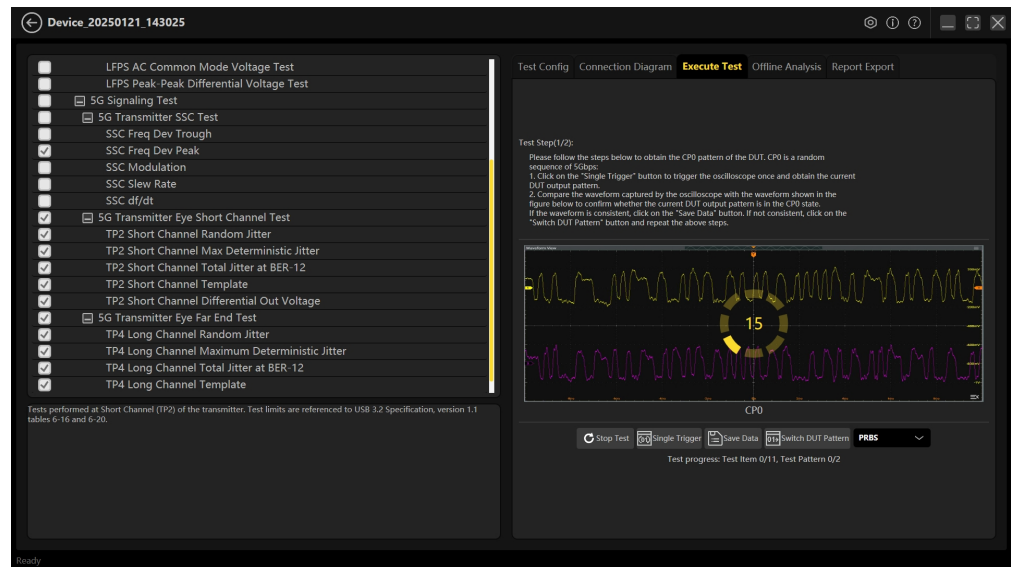


Figure 5.8 CP0

- Confirm whether the output signal sent from the DUT is CP0 pattern. If yes, click **Save Data** to save the waveform data.



- If the waveforms output from the DUT are improper, click **Switch DUT Pattern**. Then repeat the steps above until the output waveforms are proper.
- If the waveforms output from the DUT are improper, select "PRBS" and then click **Switch DUT Pattern**. Then repeat the steps above until the output waveforms are proper.

Capture CP1

Configure the oscilloscope to capture the CP1 pattern 5G test signal sent by the DUT. Then follow the "Test Step" to perform the test.

- Click **Single Trigger** to configure the oscilloscope to perform a single trigger on the CP1 pattern signal sent from the DUT.
- Compare the waveform on the oscilloscope with the test waveform shown under the Execute Test tab. You can view the waveform on the oscilloscope through the web control page to confirm that the CP1 pattern signal sent from the DUT is proper. If the output waveforms are proper, click **Save Data** to save the current waveforms of data.

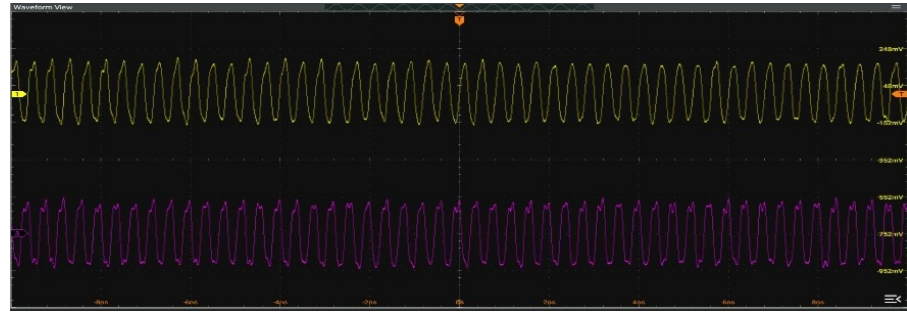


Figure 5.9 CP1

- Confirm whether the output signal sent from the DUT is CP1 pattern. If yes, click **Save Data** to save the waveform data.
- If the output waveform are improper, select "PRBS" and then click **Switch DUT Pattern**. Then repeat the steps above until the output waveforms are proper.

After the test is completed, the test report for this test is displayed automatically.

5.8.3 5G Transmitter SSC Test

If you check the checkbox of **5G Transmitter SSC Test** at the left side of the screen, click the **Execute Test** tab, then click **Start Test** to start the test. The following figure is displayed. During the test, you can stop the test any time by clicking **Stop Test**.

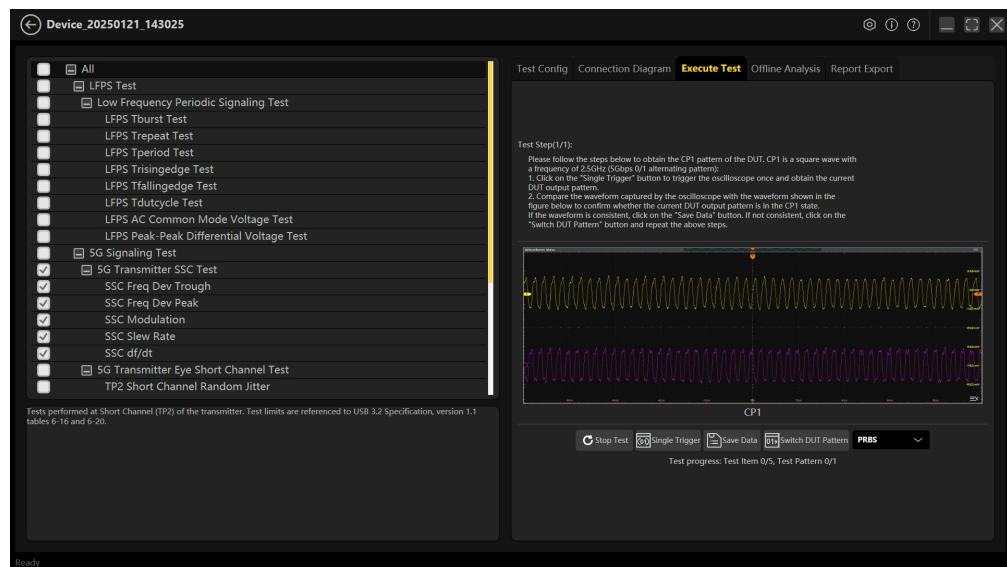


Figure 5.10 5G Transmitter SSC Test In Progress

For 5G transmitter SSC test, the DUT is required to send the CP1 pattern test signals. Configure the oscilloscope to capture the CP1 pattern 5G test signal sent by the DUT. Then follow the "Test Step" to perform the test.

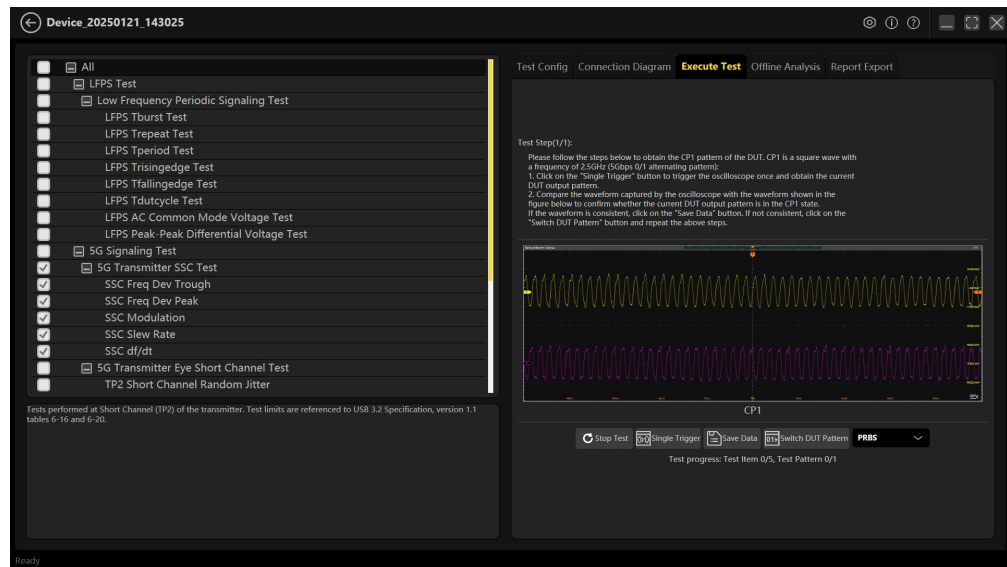


Figure 5.11 5G Transmitter SSC Test Interface

- Click **Single Trigger** to configure the oscilloscope to perform a single trigger.
- Compare the waveform on the oscilloscope with the test waveform shown under the Execute Test tab. You can view the waveform on the oscilloscope through the web control page to confirm that the CP1 pattern signal sent from the DUT is proper. If the output waveforms are proper, click **Save Data** to save the current waveforms of data.

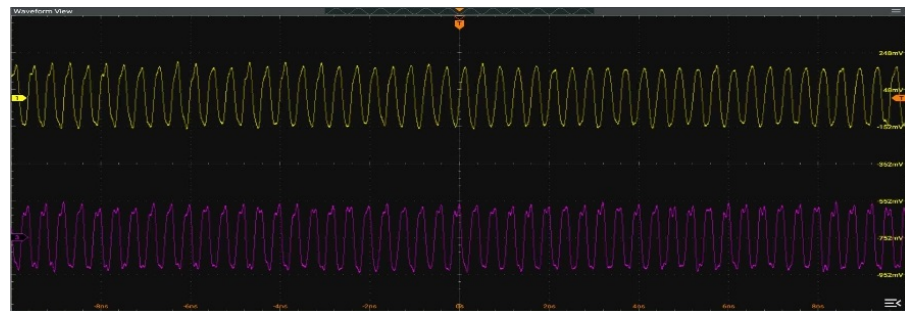


Figure 5.12 CP1

- If the output waveform are improper, select "PRBS" and then click **Switch DUT Pattern**. Then repeat the steps above until the output waveforms are proper.
- After the test is completed, the test report for this test is displayed automatically.

5.9 Offline Analysis

After completing the test, you can make an offline analysis for the saved waveform data.

Check the checkbox of the specified test item at the left side of the main interface. The test items are displayed in the "Offline Analysis" interface. Click the folder icon at the right side of the input field of the specified test item. Select the saved file from the specified path. If no data are available for the selected test item, then the analysis cannot be started.

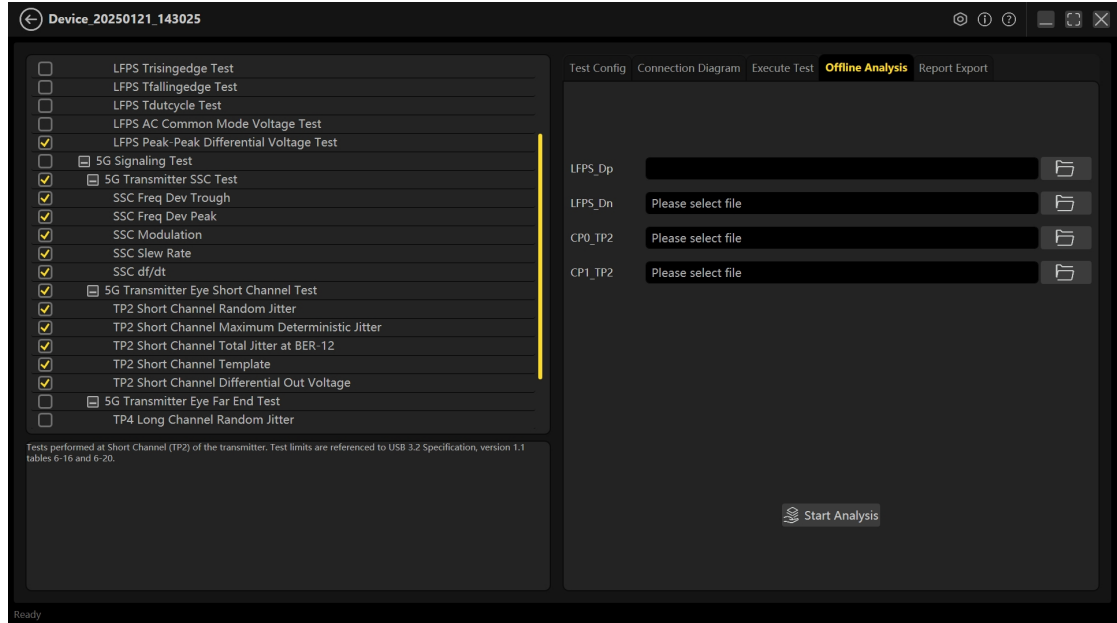


Figure 5.13 Offline Analysis Interface

- **LFPs Test:** LFPs_Dp and LFPs_Dn files are available for you to load.
- **5G Transmitter SSC Test:** The CP1_TP2 file is available for you to load.
- **5G Transmission Eye Short Channel Test:** The CP0_TP2 and CP1_TP2 files are available to be loaded.

The test is used to analyze the eye diagram of the transmitter signal. Therefore, the data file of the test point TP2 is loaded for analysis.

- **5G Transmitter Eye Far End Test:** The CP0_TP2, CP1_TP2, and CP0_TP4 files are available to be loaded.

The test is used to analyze the eye diagram of the receiver signal. Therefore, both the data of transmitter TP2 test point and that of receiver TP4 test point are loaded for comparison to make the compliance analysis.

Click **Start Analysis** to perform the analysis. After completing the analysis, the system generates the test report.

RIGOL

USB3.x Test Report

Test Configuration Details	
Application	
Application Name	Rigol USB3.x Compliance Test Application
Application Version	1.0
Oscilloscope	
Oscilloscope Model Number	
Oscilloscope Serial Number	
Oscilloscope Version	
Test Session Details	
DUT Type	Device
DUT 5G	NO
DUT Reference Clock Option	NO
DUT User Defined S-parameter File	D:\Program Files\RIGOL\RigolCTS\SSGen1_TxComp12p7dB_Embedding.s4p
Compliance Limits	USB 3.2 Specification version 1.0 (official)
Comment	0101
Test Time	2025-03-07 15:27:09

Summary of Results

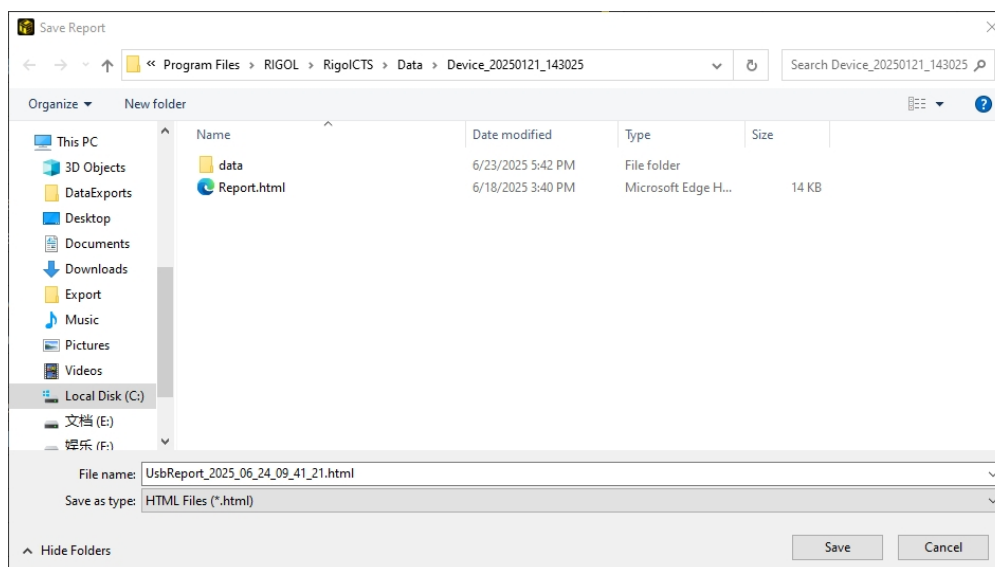
Test Statistics	
Failed	1
Passed	7
Total	8

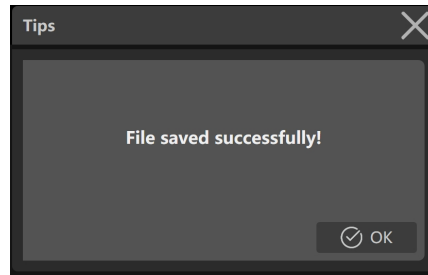
Pass	#Failed	#Trials	Test Name(click to jump)	Actual Value	Margin	Pass Limits
✓	0	3	LFPS Tburst Test	[0.884,0.948]us	35.512%	0.6us<=VALUE<=1.4us
✓	0	3	LFPS Trepeat Test	[6.969,11.043]us	11.404%	6us<=VALUE<=14us
✓	0	3	LFPS Tperiod Test	[64.143,64.175]ns	44.821%	20ns<=VALUE<=100ns
✓	0	3	LFPS Trisingedge Test	140.483ps	96.488%	VALUE<=4000ps
✓	0	3	LFPS Tfallingedge Test	125.534ps	96.862%	VALUE<=4000ps
✓	0	3	LFPS Tduty Test	49.900%	49.498%	40%<=VALUE<=60%

Figure 5.14 Test Report

5.10 To Export the Report

Click the **Export Report** tab, select the format of the file to be saved and the file path where to save the report.





6 XHSETT Tool

When performing the Host test or Hub Downstream test, use the XHSETT tool to control the USB3 host and hub to enter the compliance test mode to send the signal to be tested.

XHSETT (High Speed Electrical Test Tool) is a standard software provided by the USB-IF (USB Implementers Forum). It should be installed on the PC, and when it is launched, it will control the USB port on the current PC and make it to enter the test mode.

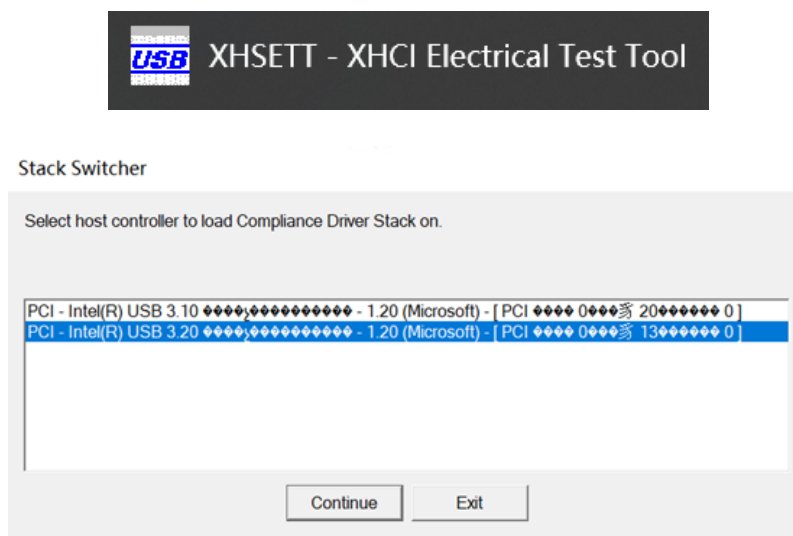
6.1 To Download and Install the Tool

Download address: <https://www.usb.org/document-library/xhsett>

Installation file: XHSETT 2.1.1.0 Installer_0.exe

6.2 To Use the XHSETT Tool

1. Double-click on the icon below to launch the XHSETT tool.



2. Click **Continue**.

Stack Switcher

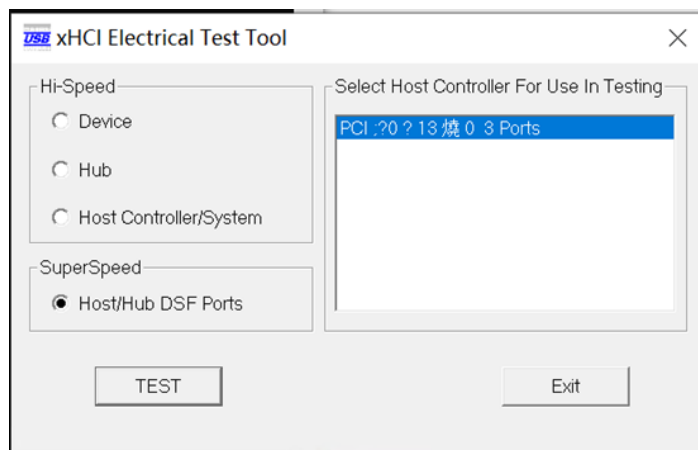
Do you want to continue with the host controller you have selected?

Click 'Continue' if so. Click 'Abort' if you would like to exit CV or choose a different host.

If you don't click anything, CV will unload the compliance driver from this host controller in 15 seconds and return to the host selection window.

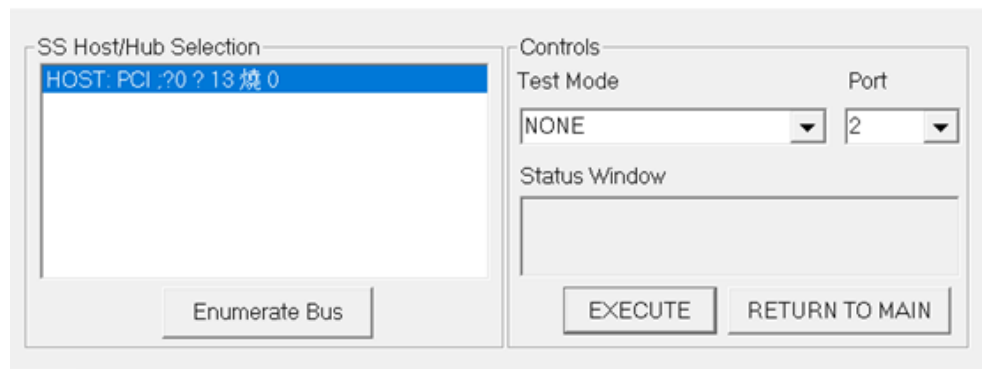
Continue

Abort

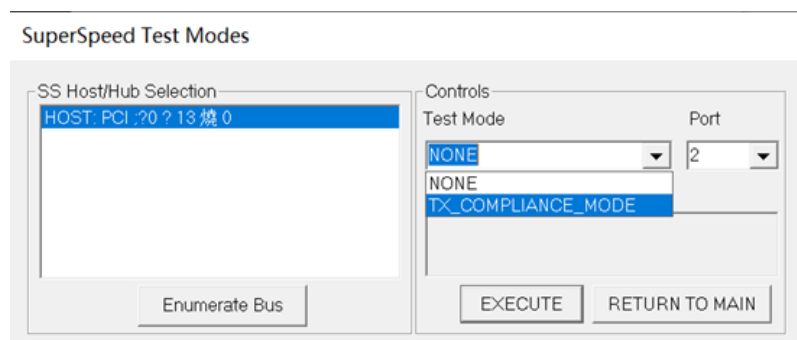


3. Select **Host/Hub DSF Ports** under **SuperSpeed**, and click **TEST**.

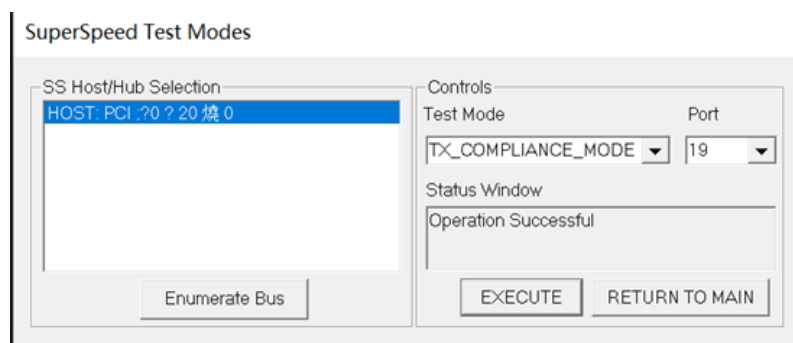
SuperSpeed Test Modes



4. Click the drop-down button of **Test Mode** to select "TX_COMPLIANCE_MODE".



5. Click the drop-down button of **Port** to select the desired Type-C port number that you want to test. For example, the port of Dell PC is 19. If you are not sure which port shall be selected, select the port number one by one until you choose the right one. Then click **EXECUTE**.



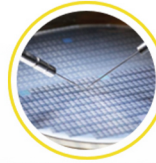
6. When the port configuration is completed, insert the HOST 1C fixture into the designated Type-C interface of the PC. If the port is properly configured, after you have inserted the HOST 1C fixture into the designated Type-C interface of the PC, the oscilloscope will capture the CP0 pattern signal.
7. Complete the test connection and perform the test according to the test step.

Boost Smart World and Technology Innovation

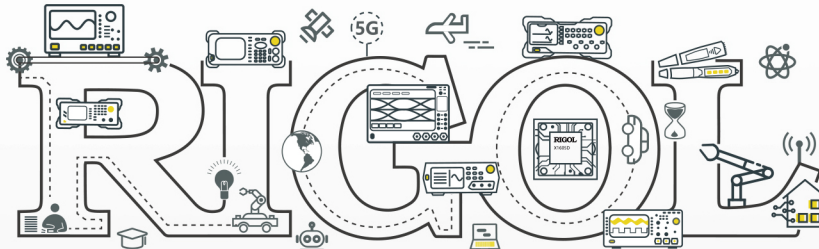
Industrial Intelligent
Manufacturing



Semiconductors



Education &
Research



Communication

System Integration



New Energy



- 5G Cellular-5G/WIFI
- UWB/RFID/ ZIGBEE
- Digital Bus/Ethernet
- Optical Communication

- Digital/Analog/RF Chip
- Memory and MCU Chip
- Third-Generation Semiconductor
- Solar Photovoltaic Cells

- New Energy Automobile
- PV/Inverter
- Power Test
- Automotive Electronics

*Provide Testing and Measuring Products
and Solutions for Industry Customers*

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