



RIGOL

MIPI D-PHY

Compliance Test

User Guide

Jul. 2025

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1 Overview of the MIPI D-PHY Compliance Test Solution

RIGOL DS70000 and DS80000 series oscilloscopes support the MIPI D-PHY compliance test, enabling you to easily configure and operate the oscilloscope to perform the test.

Technical Advantage

- Supports standard protocol, with wide test coverage
- Supports various test scenario configurations, multiple test items, capable of completing multiple tests at a time
- Supports previewing the test waveforms, convenient for you to judge whether the waveforms captured are proper and valid
- Supports generating user-defined test report in "*.pdf" or "*.html" format, with test result and measured values in it
- Provides the test devices required and user manual to guide you to perform the test

2 Document Overview

This manual introduces the following contents.

- Standard protocol supported by RIGOL MIPI D-PHY solutions
- MIPI D-PHY compliance test of the RIGOL DS80000 and DS70000 series oscilloscope
- Operation guide for performing the test for the MIPI D-PHY test items

This manual takes DS80000 series oscilloscope and PVA8700 active probe as an example to introduce RIGOL MIPI D-PHY compliance test solution.



TIP

For the latest version of this manual, download it from the official website of RIGOL (<http://www.rigol.com>).

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Format Conventions in this Manual

1. Key

The front panel key is denoted by the menu key icon. For example, indicates the "Default" key.

Default

2. Menu

The menu item is denoted by the format of "Menu Name (Bold) + Character Shading" in the manual. For example, **Test Item** indicates clicking or tapping the "Test Item" tab in the current operation interface to enter the "Test Item" menu.

3. Operation Procedures

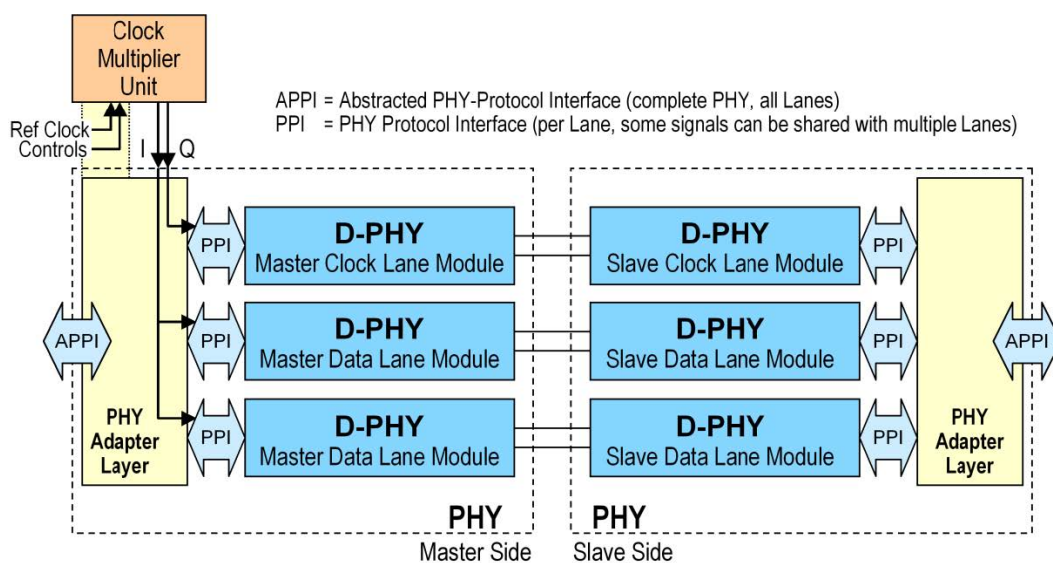
The next step of the operation is denoted by ">" in the manual. For example, **MIPI** > **Test Item** indicates that first clicking or tapping **MIPI**, then clicking or tapping **Test Item**.

3 Introduction to MIPI D-PHY Protocol

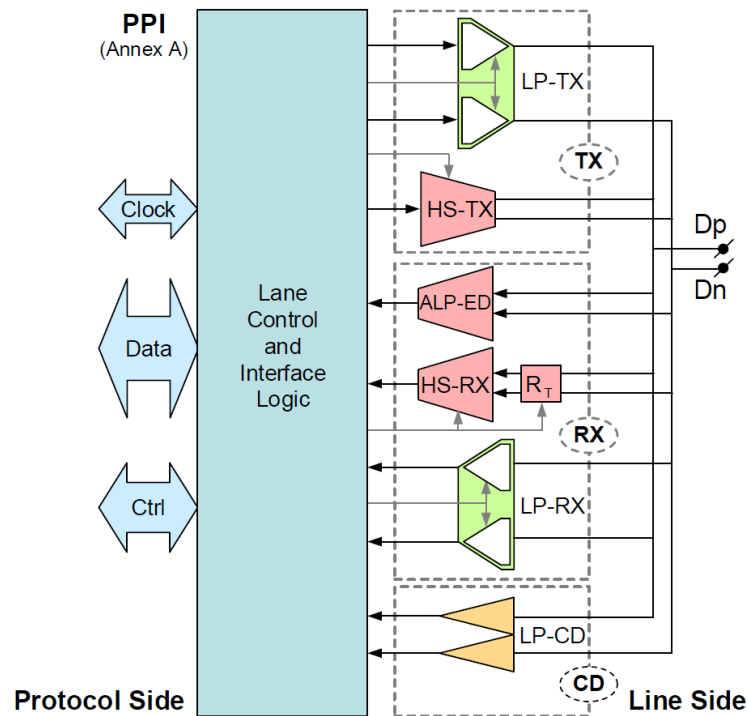
MIPI D-PHY protocol is the physical layer specifications developed by the Mobile Industry Processor Interface (MIPI) Alliance. It specifies high-speed serial interface solutions to interconnect between components inside a mobile device (e.g. Camera, display, sensor) and the processor. The D-PHY specification defines the physical characteristics, electrical characteristics, signal transmission mechanism, and etc, to realize highly efficient data transmission and meet the demands of the device for high performance and low power consumption.

3.1 D-PHY Communication Interface

D-PHY specification defines the master device and slave device, communication request from the master, clock signal, control data transmission, etc. It describes how the slave device responds to the master device, receives or sends data passively. For example, connect D-PHY interface of the processor to that of the externally connected display, the processor is considered as Master and the display is considered as Slave.



D-PHY contains at least one group of clock lanes and multiple groups of data lanes for transmission of clock and data signals. Each D-PHY channel module communicates with the counterpart D-PHY interface via two lanes (D_p and D_n).



Both the data lane and clock lane of the D-PHY have two working modes: HS (High-Speed) and LP (Low-Power).

- **HS-TX** indicates the channel is served as the signal transmitter in High-Speed mode.
- **HS-RX** indicates the channel is served as the signal receiver in High-Speed mode.
- **LP-TX** indicates the channel is served as the signal transmitter in Low-Power mode.
- **LP-RX** indicates the channel is served as the signal receiver in Low-Power mode.

This manual mainly introduces the MIPI D-PHY TX compliance test solution.

3.2 Lane Working Mode

- **High-Speed:**
 - **Data Lane** Provides differential signal (Dp/Dn) for high-speed data transmission, with the transmission rate of 80 Mbps to 2.5 Gbps, requiring to meet strict timing requirements, used in high-speed transmission of images and videos.

- **Clock Lane** Provides differential clock signal (Clkp/Clkn) for high-speed transmission. It can synchronize with the data lane in transmission. It supports the transmission rate of 80 Mbps to 2.5 Gbps, providing sync clock for high-speed data transmission.
- **Low-Power:**
 - **Data Lane** Single-ended signal (Dp/Dn independently driven), transmission rate <10 Mbps, multiple working modes
 - **Clock Lane** Single-ended signal (Clkp/Clkn independently driven), often used in controlling the mode switch.

In the non-transmission period, the clock lane is disabled and enter the ULPS (Ultra-Low Power State) state to save power.

The data lane has multiple operating states in LP mode.

- Control Mode: controls the data lane communication direction and state switching.
- Escape Mode: a special mode of operation for data lanes using Lower-Power state. Includes the following actions:
 - LPDT: Low-Power Data Transmission.
 - ULPS: Ultra-Low Power State.
 - Trigger: the mechanism to send a flag to the protocol at the receiving side, on request of the protocol at the transmitting side.

The PHY in Escape mode shall apply Spaced-One-Hot bit encoding for asynchronous communication. Therefore, operation of a data lane in this mode does not depend on the clock lane. For data lanes, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. The following table lists all currently available Escape mode commands and actions.

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Table 8 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

3.3 Channel State Pattern

The channel state can be determined by the level of the pins to which the data lane and clock lane of the DUT transmitter are connected for the MIPI D-PHY compliance test.

Table 2 Lane State Descriptions

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A, Note 1	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 1	N/A, Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note 2

Note:

1. During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.
2. If LP-11 occurs during Escape Mode the Lane returns to Stop state (Control mode LP-11).

In High-Speed mode, the differential signals are output from the Dp and Dn pins. Two high-speed lane states:

- **HS-0:**

In HS mode, Dp is considered as the positive side and Dn as the negative side. The Dp Line indicates the low level, and the Dn line indicates the high level.

In HS burst mode, the differential signal state is Differential-0 ($V_{Dp} < V_{Dn}$);

- **HS-1:**

In HS mode, Dp is considered as the positive side and Dn as the negative side. The Dp Line indicates the high level, and the Dn line indicates the low level.

In HS burst mode, the differential signal state is Differential-1 ($V_{Dp} > V_{Dn}$);

In Low-Power mode, the Dp and Dn lines are independent of each other. Four Low-Power Lane states:

- **LP-00:**

In LP mode, Dp line is 0, and Dn line is 0.

In LP Control mode, the lane is in Bridge state, the transition state from LP, HS, or Escape

In LP Escape mode, the lane is in Space state, indicating the interval in data transmission. Each Mark-1 or Mark-0 is followed by a Space state, which is used to provide clock signal in the successive Mark states.

- **LP-01:**

In LP mode, Dp line is 0, and Dn line is 1.

In LP Control mode, the lane is in HS-Rqst state, indicating requesting to transition to HS mode.

In LP Escape mode, the lane is in Mark-0 state, indicating logic 0.

- **LP-10:**

In LP mode, Dp line is 1, and Dn line is 0.

In LP Control mode, the lane is in LP-Rqst state, indicating requesting to transition from HS to LP or Escape mode.

In LP Escape mode, the lane is in Mark-1 state, indicating logic 1.

- **LP-11:**

In LP mode, Dp line is 1, and Dn line is 1.

In LP Control mode, the lane is in Stop state, indicating that any mode must start from Stop state and ends with Stop state.

4 Test Device

The following table lists the devices used in the MIPI D-PHY electrical tests.

Table 4.1 Devices Required

Device	Description
DUT	Product under test or chip and module under test
Digital Oscilloscope	Supports the MIPI D-PHY compliance test Supports the eye diagram and jitter function BW $\geq$ 4 GHz; 4-CH
Active Probe	BW: $\geq$ 4 GHz (x4)
Test Fixture	Low-power capacitive load board: 50pF C _{LOAD}
	Reference Termination Board (RTB)
SMA Cable	4, used to connect the device interface

The following table lists the recommended devices.

Table 4.2 Recommended Devices

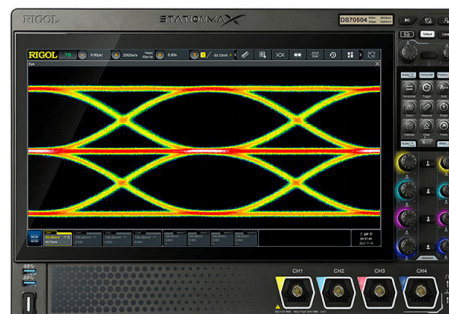
Device	Model
Digital Oscilloscope	RIGOL DS80000 series digital oscilloscope equipped with - MIPI D-PHY compliance test option - BNC probe adapter (x4)
	RIGOL DS70000 series digital oscilloscope equipped with MIPI D-PHY compliance test option
Active Probe	RIGOL PVA8700 active probe (x4) Solder-in single-ended or differential probe head
RTB	Model: UNH-IOL RTB V3.3 Proto Board (x1) Note: The RTB board is only used for chip-level testing.
CLoad Board	Model: MIPI D-PHY Capacitive Load (CLoad) Board V1 (x1) Note: CLoad board is only used for Escape mode testing.

4.1 Digital Oscilloscope and Probe

To enable the MIPI D-PHY compliance test, install the DPHYC option on the RIGOL DS80000 or DS70000 series digital oscilloscope.



DS80000 Series Digital Oscilloscope



DS70000 Series Digital Oscilloscope

DS80000 series digital oscilloscope requires to use the probe adapter, which is equipped with two standard configuration of precision BNC adapters (3.5 mm-to-BNC, 50 Ω).



BNC Adapter Input 50 Ω



High Impedance Adapter (1M Ω)

RIGOL PVA8700 Active Probe



PVA8700 Active Probe

Four types of probe heads:

- Hand-held Differential Probe Head
- Hand-held Single-ended Probe Head
- Solder-in Differential Probe Head
- Solder-in Single-ended Probe Head

4.2 Test Fixture

When performing the MIPI D-PHY compliance test for some DUTs, a test fixture is required. It can automatically match the load condition specified in the Specification based on the captured MIPI D-PHY signal waveform characteristics. It can auto switch between 100 Ω differential load and 50 pF capacitive load to meet the test scenarios for LP and HS modes.

50pF C_{LOAD} Fixture

In the MIPI D-PHY compliance test, the 50pF C_{LOAD} (Capacitive load) fixture is an important tool used to emulate the actual receiver load, including the capacitive load and impedance match, etc. to ensure the performance of the DUT in the actual application.

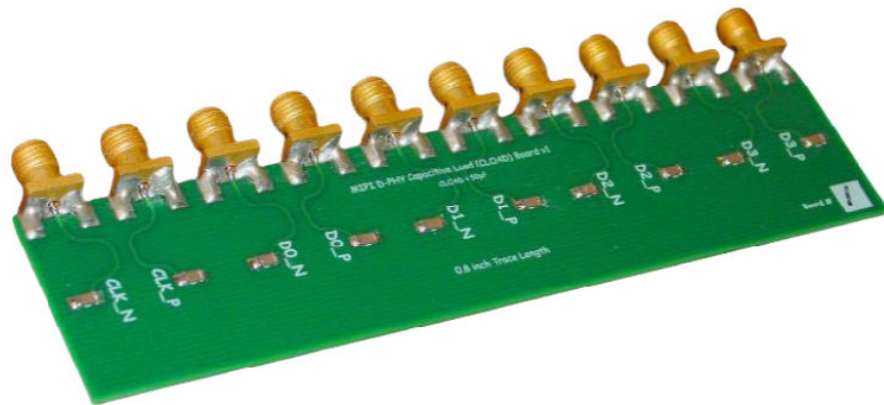


Figure 4.1 50pF C_{LOAD} Fixture



NOTE

50pF C_{LOAD} test fixture is only available in the test items of Group 1 and Group 2 of DUT LP mode.

Reference Termination Board (RTB)

The RTB (Reference Termination Board) fixture is an important tool used in the MIPI D-PHY compliance test. It can be mainly used to emulate the actual receiver load, including impedance match and signal reflection, etc. to ensure that the DUT can work normally in various conditions. In the development and debugging stage, the RTB fixture can help engineers find out and resolve the potential problems, ensuring the reliability and stability of the devices.

The MIPI D-PHY RTB from the University of New Hampshire InterOperability Lab (UNH-IOL) is recommended. The UNH-IOL works closely with the MIPI Alliance (standard body for MIPI) and has developed a testing program/fixtures/boards to meet the unique needs of the mobile industry (including the D-PHY RTB).

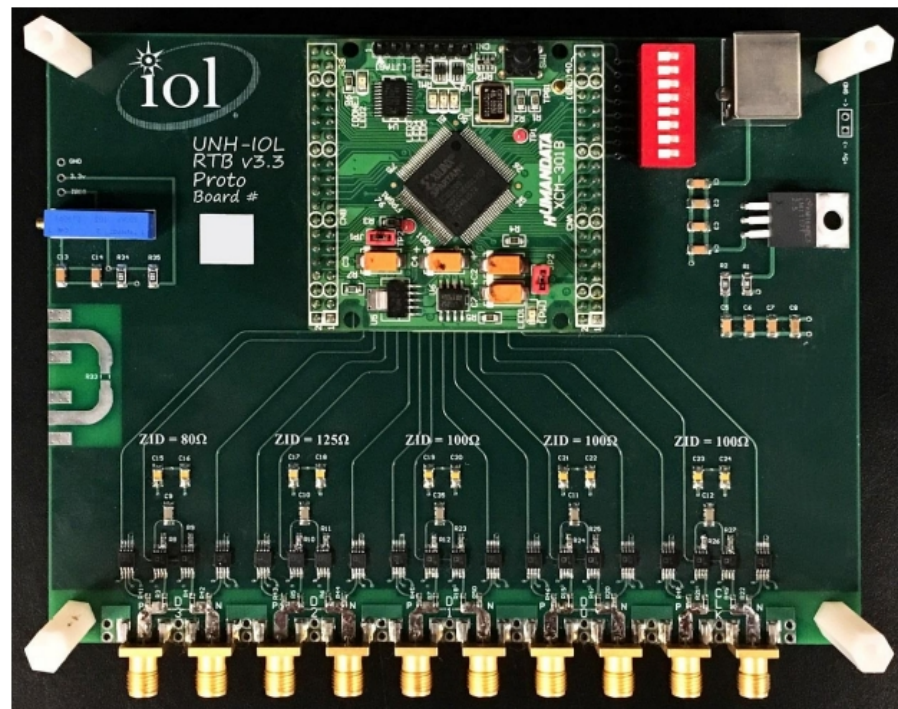


Figure 4.2 Reference Termination Board (RTB)

RTB has

- One clock lane
- Three data lanes with $Z_{ID} = 100 \Omega$
- One data lane with $Z_{ID} = 80 \Omega$
- One data lane with $Z_{ID} = 125 \Omega$



NOTE

In the actual measurement, we usually test on the RTB data lane with $Z_{ID} = 80 \Omega$. However, to comply with the D-PHY Specification, we use the data lane with $Z_{ID} = 125 \Omega$ or $Z_{ID} = 80 \Omega$ for some extreme cases of the load.

5 To Calibrate the Digital Oscilloscope and the Probe

If the oscilloscope has not used or replaced the probe for a long time, calibrate the oscilloscope and the probe first before use. This chapter takes DS80000 digital oscilloscope and PVA8000 probe as an example to introduce the calibration method.

For detailed information about DS80000 digital oscilloscope, refer to *DS80000 User Guide*. For detailed information about PVA8000 probe, refer to *PVA8000 Active Probe User Guide*.

5.1 To Calibrate the Digital Oscilloscope

The self-calibration program can quickly make the oscilloscope to work in an optimal state to get the precise measurement results. You can perform the self-calibration at any time, especially when the variation of the ambient environment is above $\pm 5^{\circ}\text{C}$. Make sure that the oscilloscope has been warmed up or operating for more than 30 minutes before the self-calibration.

In the function navigation menu, click or tap **Utility** > **SelfCal**, the following self-calibration interface is shown below.

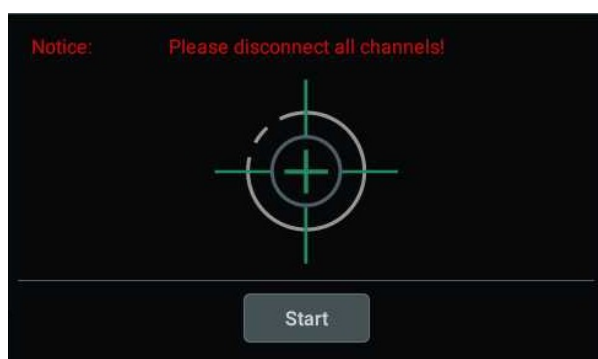


Figure 5.1 Self-calibration Interface

Click or tap **Start**, and then the oscilloscope will start to execute the self-calibration program. After completing the self-calibration, click or tap **Close** to close the self-calibration window.

5.2 To Calibrate the Active Probe

If the oscilloscope works with an active probe, the probe ratio cannot be modified and you need to calibrate the probe.

For example, connect the PVA8000 probe to the analog channel of the oscilloscope. Note that no signal is connected to the probe. After the oscilloscope recognizes the

probe, the probe setting interface is displayed, as shown in the following figure. Slide to select the desired channel (CH1-CH4), or click/tap the desired channel tab to switch to probe setting interface of the specified channel.

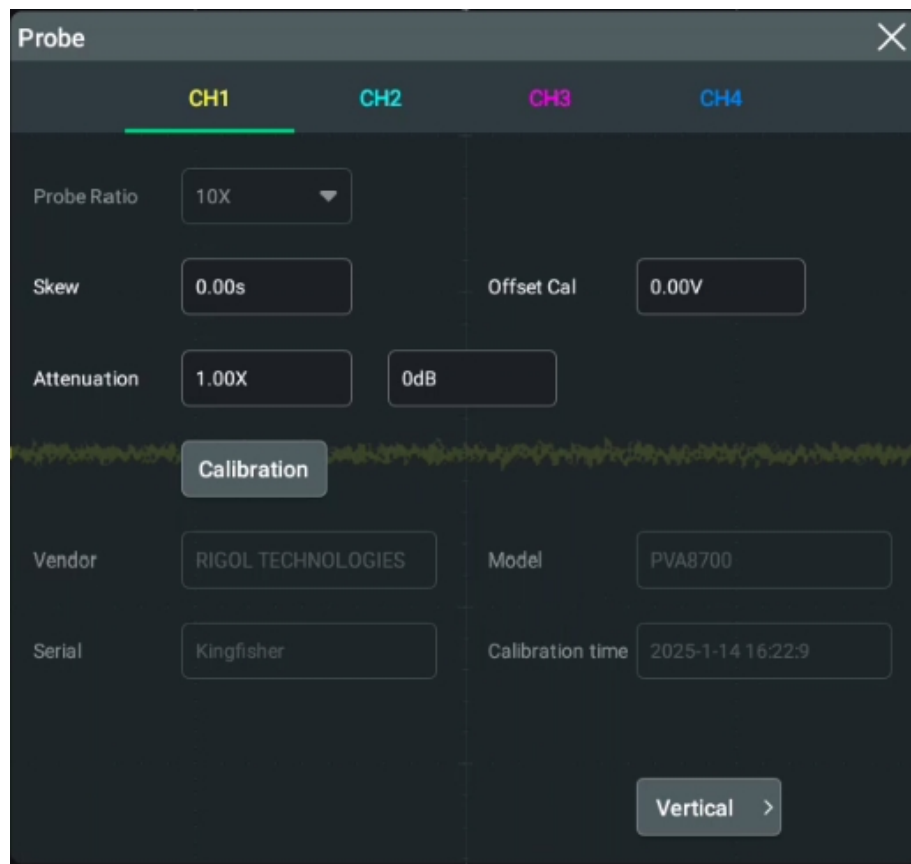


Figure 5.2 Active Probe Calibration Menu

Click or tap **Calibration**, then the oscilloscope auto calibrates the probe. The calibration lasts about 80 to 90 seconds. After completing the probe calibration, the calibration results information that notifies you of the completion of the probe calibration or failure of the probe calibration is displayed.

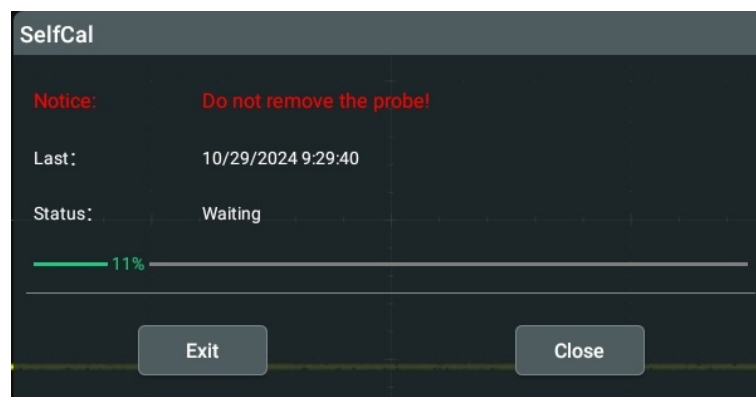


Figure 5.3 Probe Calibration Window

The specifications of the PVA8000 series active probe depends on the probe calibration. After completing the calibration, the DC gain, offset calibration, and offset gain will all be calibrated. As the offset calibration value of the PVA8000 series active probe is provided by the BNC module, after completing the calibration for the first time of use, you do not need to calibrate it again for the next time.

Notice

If you select another channel, you need to calibrate the probe again.

5.3 To Calibrate the Channel Skew

PVA8000 series probe supports both the hand-held and solder-in probe head. Using different types of probe head does not affect the calibration results. When performing the compliance test on the DUT, use the solder-in single-ended or differential probe head. For ease of operation, hand-held single-ended probe head is recommended in calibration. The following section takes CH1 and CH2 as an example to introduce the skew calibration for the specified channel.

1. Connect the oscilloscope with the probe

Connect two equal-length PVA8700 probes to CH1 and CH2 respectively. Connect the ground cable of the probe to GND of the oscilloscope. Use the SMA cable to connect to the AUX Out connector of the oscilloscope to output the fast-edge signal. Connect the probe tip of the two PVA8700 probes to the signal output.

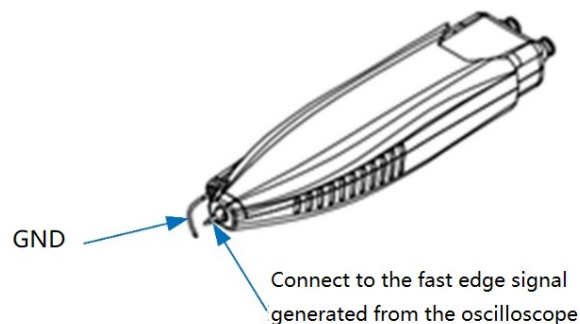


Figure 5.4 Probe Calibration Connection Diagram

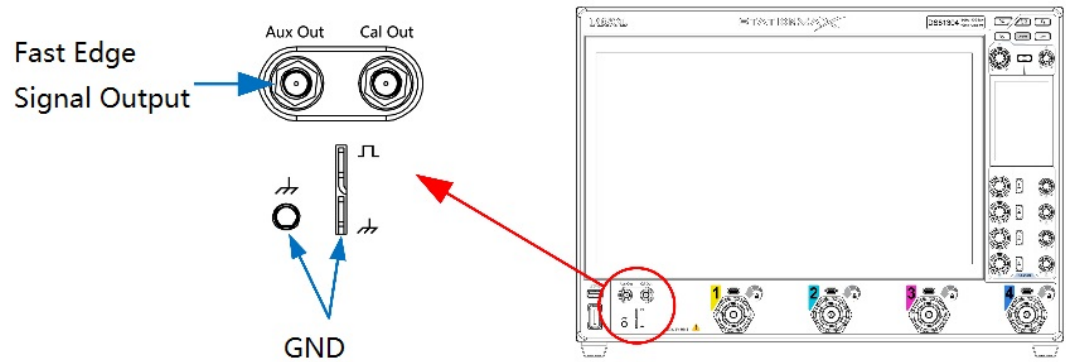


Figure 5.5 Digital Oscilloscope Calibration Connection Diagram

2. Configure the oscilloscope to output the fast edge signal

In the function navigation menu, click or tap **Utility** > **Demo Signals** to enter the demo signal setting menu. Click or tap ON for **FastEdge Output** to enable the oscilloscope to output the standard fast edge signal, as shown in the figure below.

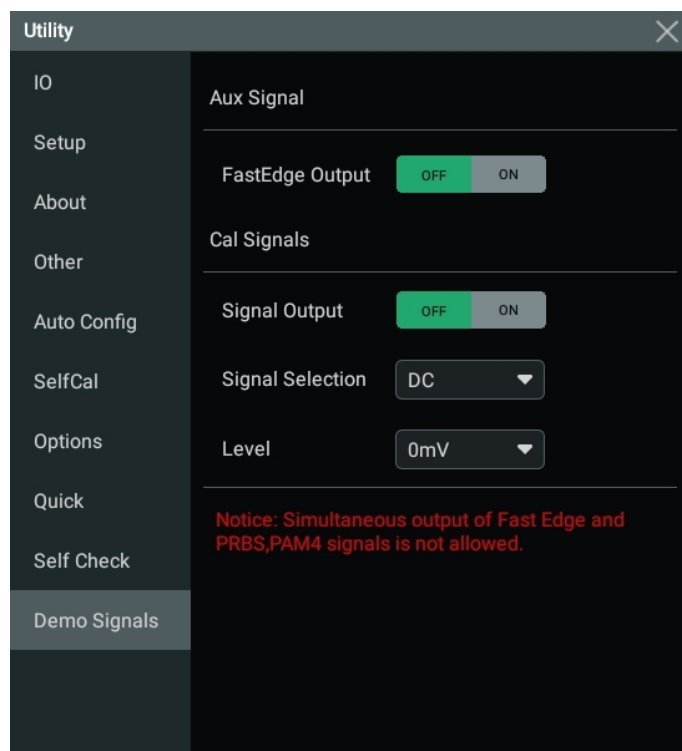


Figure 5.6 Fast Edge Output Setting

3. Configure the oscilloscope to capture the fast edge signal of CH1 and CH2

In the Vertical system menu, set the impedance of CH1 and CH2 to 50 Ω .

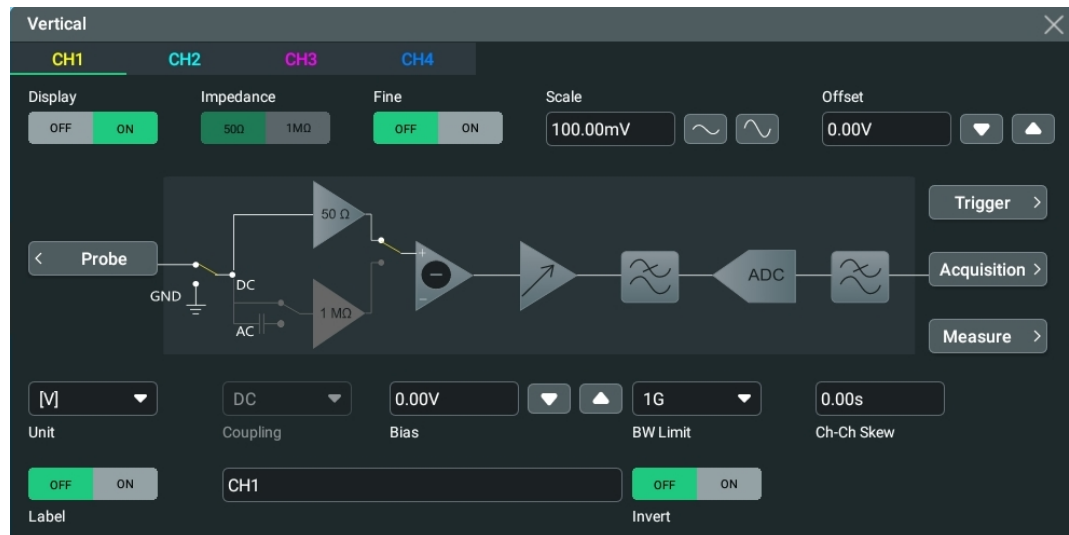
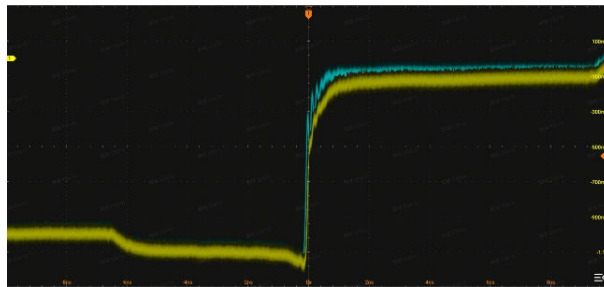


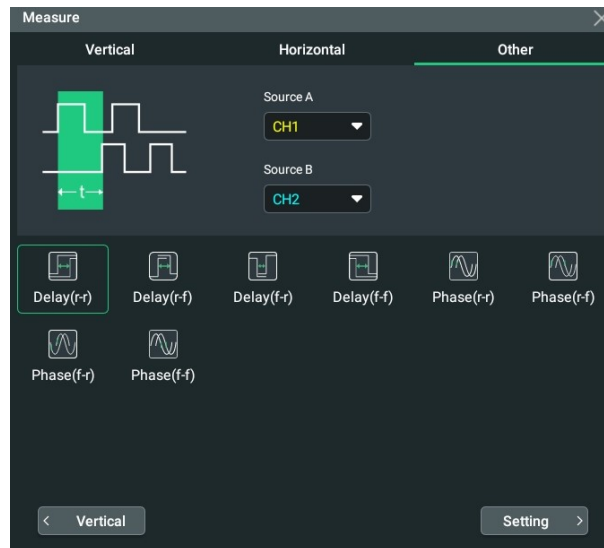
Figure 5.7 Vertical System Menu

In the function navigation menu, click or tap **Auto**. Then the waveforms of the fast edge signals of CH1 and CH2 are displayed on the screen.

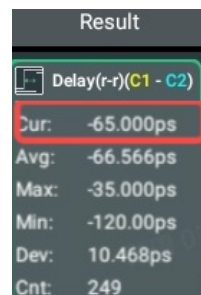


4. Measure the channel skew between CH1 and CH2

In the Measure menu, click or tap **Other** > **Delay** to enable the channel delay between CH1 and CH2.



The measurement results are displayed at the right side of the screen under the "Result" list, as shown in the figure below.



5. Take CH1 as a reference to calibration the channel skew between CH1 and CH2

Assume that the skew is 60 s, then set the channel delay of CH2 in the Vertical system menu to 60 s. If the skew is -60 s, then set the skew to -60 s.

6. Repeat Step 4-5 until the measured delay result is within ± 10 ps.

7. Repeat the above-mentioned operations to take CH1 as a reference to complete the channel skew between CH1 and CH3. The same operation can be done for the channel skew calibration between CH2 and CH4 by taking CH2 as a reference.

6 MIPI D-PHY Compliance Test

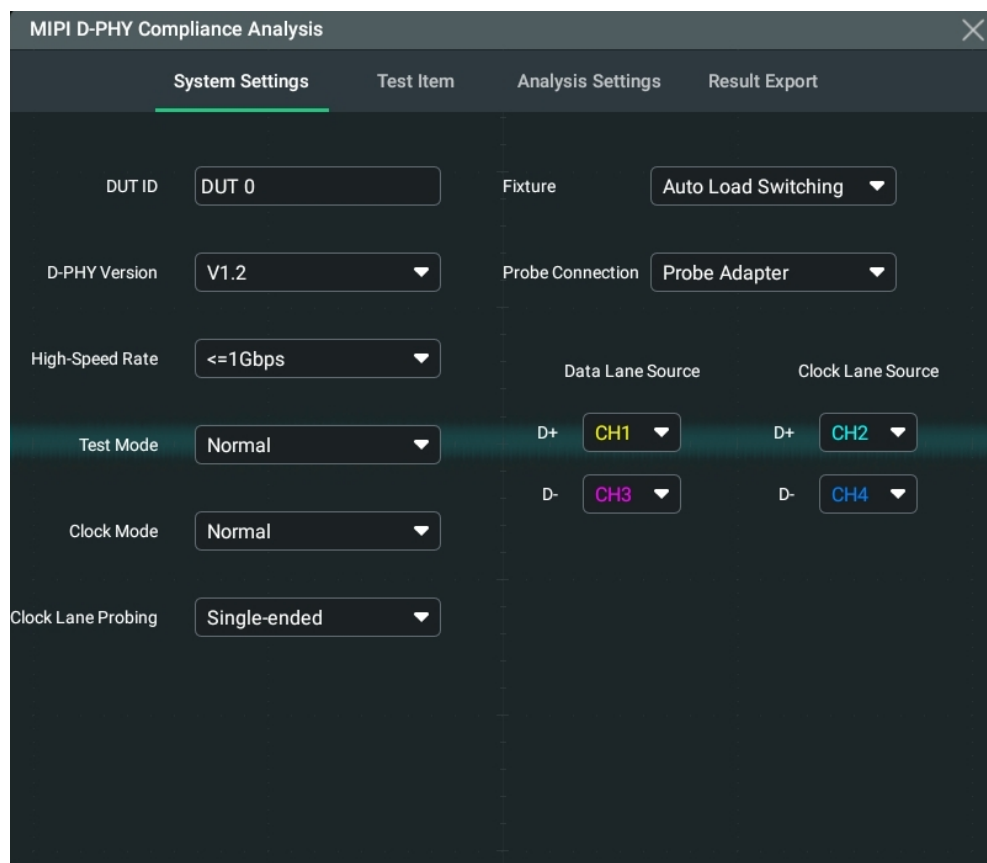
DS70000 and DS80000 series oscilloscopes support MIPI D-PHY compliance test. It is available to use when you purchase the DPHYC option and activate the option. For detailed functions of the DS70000 or DS80000 series digital oscilloscope, refer to *DS70000 User Guide* and *DS80000 User Guide*.

This manual takes DS80000 series oscilloscope as an example to introduce RIGOL MIPI D-PHY compliance test solution.

In the main interface of the oscilloscope, click or tap  > **MIPI** to enter the "MIPI D-PHY Compliance Analysis" interface.

6.1 System Settings

Click or tap the "System Settings" tab to configure the test, as shown in the figure below.



MIPI D-PHY Compliance Analysis

System Settings Test Item Analysis Settings Result Export

DUT ID: DUT 0 Fixture: Auto Load Switching ▼

D-PHY Version: V1.2 ▼ Probe Connection: Probe Adapter ▼

High-Speed Rate: <=1Gbps ▼

Data Lane Source: D+ CH1 ▼ D- CH3 ▼

Clock Lane Source: D+ CH2 ▼ D- CH4 ▼

Test Mode: Normal ▼

Clock Mode: Normal ▼

Clock Lane Probing: Single-ended ▼

Figure 6.1 System Settings Interface

DUT ID

Inputs the ID of the DUT. It is only used in test report.

D-PHY Version

Three versions of *MIPI Alliance Specification for D-PHY* are available: V1.0, V1.1, and V1.2.

The test items are a bit different for different versions. For example, in D-PHY V1.2, Test 1.5.5 and Test 1.5.6 are included; in D-PHY V1.0, Test 1.4.18 is not included.

High-Speed Rate

The available choices for high-speed rate are as follows: ≤ 1 Gbps, > 1 Gbps and ≤ 1.5 Gbps, > 1.5 Gbps and ≤ 2.5 Gbps. The ranges of the high-speed rate for different "D-PHY" versions are different. Selecting a different high-speed rate may result in different pass/fail standards for some test items, thus affecting the pass/fail results of the test report. However, this does not affect the actual measurement value of each test item.

Test 1.5.5 and Test 1.5.6 are only applicable to high rate above 1.5 Gbps.

Test Mode

- **Normal:** supports test items of Group3, Group4, Group5, and Eye Diagram Test.
- **Escape:** supports test items of Group1 and Group2.
- **Normal+Escape:** supports test items of Group1 through Group5 and Eye Diagram Test.
- **Continuous Data:** this mode is the standard working mode not specified in MIPI D-PHY Specification. It is only available for the specified test items when the data lane and clock lane of the DUT output continuous high-speed signal. This mode only supports some test items of Group3 through Group5 and test items of Eye Diagram Test.

Clock Mode

- **Continuous:**

During the data transmission on the data lane, whatever the data lane is in LP or HS state, the clock lane always stays in HS state and will not change to LP state.

If "Continuous" is selected for the clock mode, you can select "Single-ended" or "Differential" as the clock mode probing.

- **Normal:**

During the data transmission on the data lane, the data lane enters the LP state, and the clock lane also switches to LP state. Before the data lane enter the HS

state again, the clock lane needs to switch to the HS state, therefore, the clock is normal.

If "Normal" is selected for the clock mode, you can only select "Single-ended" clock mode probing.

The test items are different under a different clock mode. The continuous clock mode is not applicable to Group2, Test 1.4.1 through Test1.4.3, Test 1.4.13 through Test1.4.16, and Test 1.5.1 through Test 1.5.2. When you select "Continuous Data" as the test mode, only "Continuous" is available for the Clock Mode.

Fixture Setting

Selects whether to use the test fixture and enable auto switching or manual switching based on the actual test scenarios.

- **Auto Load Switching:**

If you select this mode, after starting test, the oscilloscope prompts you to connect via the fixture, then display the connection diagram and operation procedures for you to perform the test. The actual test results will not be affected. This mode is generally adopted for the test fixture that is able to handle the automatic switching of the required termination load.

- **Manual Load Switching:**

If you select this mode, after starting test, the oscilloscope prompts you the connection diagram that does not require the fixture and operation procedures for you to perform the test. The actual test results will not be affected. It is generally used in bare chip test where the termination load is required to be switched manually.

Probe Connection

- **Direct Connection:** For DS70000 series digital oscilloscope, the probe is connected directly to the oscilloscope.
- **Connect the probe via the probe adapter:** For DS80000 series oscilloscope, the probe is connected to the oscilloscope via the probe adapter.

Clock Lane Probing

- **Single-ended:** selects the single-ended probe. The waveforms displayed on the oscilloscope show the variations of the voltage of the signal under test over time in relative to the GND.

When "Single-ended" is selected for "Clock Lane Probing", the available choices for clock mode are "Continuous" and "Normal".

- **Differential:** selects the differential probe. The waveforms displayed on the oscilloscope show the variations of the voltage difference between two input signals over time.

When "Differential" is selected for "Clock Lane Probing", the available choice for "Clock Mode" is "Continuous" only.

The differential clock lane probing is not applicable to Group2, Test 1.4.1 through Test 1.4.3, Test 1.4.6 through Test 1.4.10, Test 1.4.13 through Test 1.4.16, and Test 1.5.1 through Test 1.5.2.

The choices for clock lane probing shall be consistent with the actual test connection. To view the connection diagram for different types of probe, refer to [Test Connection](#).

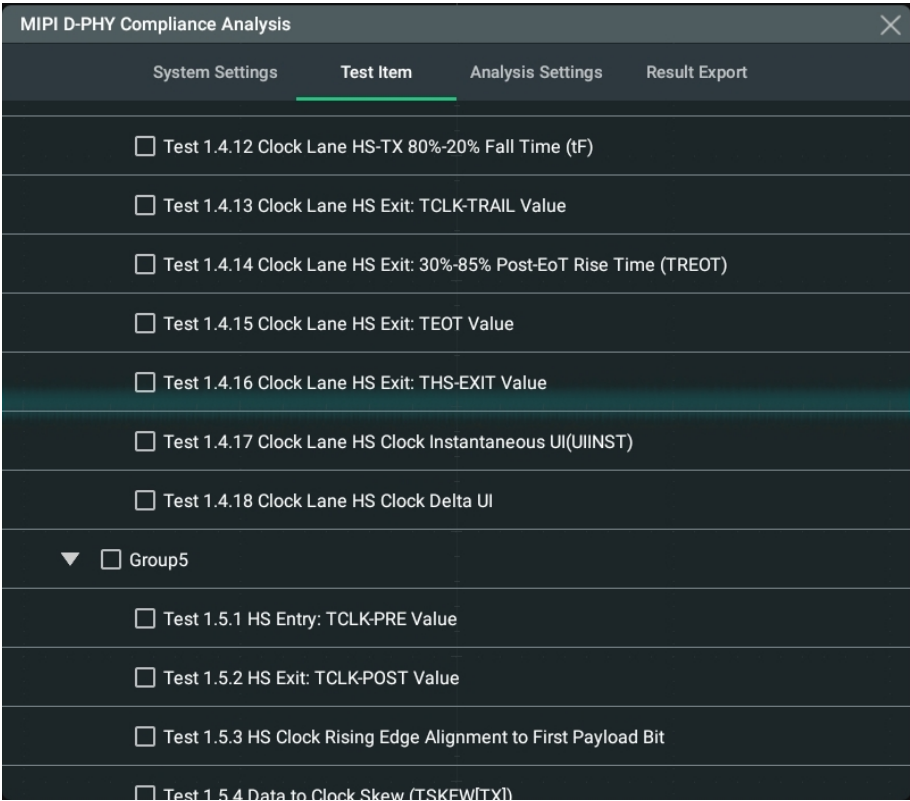
Set the Source

- **Data Lane Source:** Click or tap the drop-down button of **D+** or **D-** under **Data Lane Source** to select the desired source from the drop-down list.
- **Clock Lane Source:** Click or tap the drop-down button of **D+** or **D-** under **Clock Lane Source** to select the desired source from the drop-down list.

By default, CH1 and CH3 are considered as a pair, CH2 and CH4 are considered as another pair. Two adjacent channels such as CH1 and CH2, CH2 and CH3 are not supported as one pair. When you select differential clock lane probing, select CH2 or CH4.

6.2 Test Item

After completing the configurations in the "System Settings" tab, click or tap the **Test Item** tab to enter the test item menu, as shown in the figure below.



Check the checkbox of the specified test item to select the desired test item.

6.2.1 Test Items of Group1

Group1 Data Lane LP-TX Signaling Test includes the following test items.

Test Item	Description
Test 1.1.1	Data Lane LP-TX Thevenin Output High Level Voltage (V_{OH})
Test 1.1.2	Data Lane LP-TX Thevenin Output Low Level Voltage (V_{OL})
Test 1.1.3	Data Lane LP-TX 15%-85% Rise Time (T_{RLP})
Test 1.1.4	Data Lane LP-TX 15%-85% Fall Time (T_{FLP})
Test 1.1.5	Data Lane LP-TX Slew Rate vs. CLOAD ($\delta V/\delta t_{SR}$)
Test 1.1.6	Data Lane LP-TX Pulse Width of Exclusive-OR Clock ($T_{LP-PULSE-TX}$)
Test 1.1.7	Data Lane LP-TX Period of Exclusive-OR Clock ($T_{LP-PERTX}$)

Configuration Requirements

To perform the test items of Group1, configure the following parameters in the **System Settings** tab for the MIPI compliance test.

- Select "Escape" or "Normal+Escape" from the drop-down button of "Test Mode".
- Other parameters are not required to be set, leaving them as default settings.

Test Connection

The available test connections for Group1 test items are as follows:

- For connecting via the 50pF C_{LOAD} test fixture, refer to descriptions in [Figure 7.1](#).
- For connecting data lane only, refer to [Figure 7.6](#).

6.2.2 Test Items of Group2

Group2 Clock Lane LP-TX Signaling Test includes the following test items.

Test Item	Description
Test 1.2.1	Clock Lane LP-TX Thevenin Output High Level Voltage (V_{OH})
Test 1.2.2	Clock Lane LP-TX Thevenin Output Low Level Voltage (V_{OL})
Test 1.2.3	Clock Lane LP-TX 15%-85% Rise Time (T_{RLP})
Test 1.2.4	Clock Lane LP-TX 15%-85% Fall Time (T_{FLP})
Test 1.2.5	Clock Lane LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)

Configuration Requirements

To perform the test items of Group2, configure the following parameters in the **System Settings** tab for the MIPI compliance test.

- Select "Escape" or "Normal+Escape" from the drop-down button of "Test Mode".
- Click or tap the drop-down button of **Clock Mode** to select "Normal".
- Click or tap the drop-down button of **Clock Lane Probe** to select "Single-ended".
- Other parameters are not required to be set, leaving them as default settings.

Connection

The available test connections for Group2 test items are as follows:

- For connecting via the 50pF C_{LOAD} test fixture, refer to descriptions in [Figure 7.1](#).
- For single-ended probing for clock lane, refer to descriptions in [Figure 7.7](#).

6.2.3 Test Items of Group3

Group3 Data Lane HS-TX Signaling Test includes the following test items.

Test Item	Description
Test 1.3.1	Data Lane HS Entry: Clock Lane TLPX Value
Test 1.3.2	Data Lane HS Entry: THS-PREPARE Value
Test 1.3.3	Data Lane HS Entry: THS-PREPARE+THS-ZERO Value
Test 1.3.4	Data Lane HS-TX Differential Voltages ($V_{OD(0)}$, $V_{OD(1)}$)
Test 1.3.5	Data Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})
Test 1.3.6	Data Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$)
Test 1.3.6	Data Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DN)}$)
Test 1.3.7	Data Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}$, $V_{CMTX(0)}$)
Test 1.3.8	Data Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$)
Test 1.3.9	Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($\Delta V_{CMTX(LF)}$)
Test 1.3.10	Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{CMTX(HF)}$)
Test 1.3.11	Data Lane HS-TX 20%-80% Rise Time (t_R)
Test 1.3.12	Data Lane HS-TX 80%-20% Fall Time (t_F)
Test 1.3.13	Data Lane HS Exit: THS-TRAIL Value
Test 1.3.14	Data Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})
Test 1.3.15	Data Lane HS Exit: TEOT Value
Test 1.3.16	Data Lane HS Exit: THS-EXIT Value

Configuration Requirements

To perform the test items of Group3, configure the following parameters in the **System Settings** tab for the MIPI compliance test.

- Select "Escape", "Normal+Escape", or "Continuous Data" from the drop-down button of **Test Mode**.
- Other parameters are not required to be set, leaving them as default settings.

Connection

Select "Normal" or "Normal+Escape" from the drop-down button of **Test Mode**.

- For connecting via the RTB fixture, refer to descriptions in *To Connect via the RTB Fixture*.
- For connecting the clock lane and data lane, refer to descriptions in *To Connect the Clock Lane and Data Lane*.

When you select "Continuous Data" as the clock mode, refer to connection methods in *Continuous Data Test Connection*.

6.2.4 Test Items of Group4

Group 4 Clock Lane HS-TX Signaling Requirements includes the following test items.

Test Item	Description
Test 1.4.1	Clock Lane HS Entry: Clock Lane TLPX Value
Test 1.4.2	Clock Lane HS Entry: TCLK-PREPARE Value
Test 1.4.3	Clock Lane HS Entry: TCLK-PREPARE+TCLK-ZERO Value
Test 1.4.4	Clock Lane HS-TX Differential Voltages ($V_{OD(0)}$, $V_{OD(1)}$)
Test 1.4.5	Clock Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})
Test 1.4.6	Clock Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$)
Test 1.4.6	Clock Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DN)}$)
Test 1.4.7	Clock Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}$, $V_{CMTX(0)}$)
Test 1.4.8	Clock Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$)
Test 1.4.9	Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($\Delta V_{CMTX(LF)}$)
Test 1.4.10	Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{CMTX(HF)}$)

Test Item	Description
Test 1.4.11	Clock Lane HS-TX 20%-80% Rise Time (t_R)
Test 1.4.12	Clock Lane HS-TX 80%-20% Fall Time (t_F)
Test 1.4.13	Clock Lane HS Exit: TCLK-TRAIL Value
Test 1.4.14	Clock Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})
Test 1.4.15	Clock Lane HS Exit: TEOT Value
Test 1.4.16	Clock Lane HS Exit: THS-EXIT Value
Test 1.4.17	Clock Lane HS Clock Instantaneous UI (UI_{INST})
Test 1.4.18	Clock Lane HS Clock Delta UI (ΔUI)

Configuration Requirements

The configurations for different test items of Group4 are different. As the clock signal are output continuously in continuous data mode, the clock lane will not be switched between HS and LP state, thus unable to perform tests concerning clock lane state switch. Therefore, some of the test items are required to be performed for non-continuous signal.

To perform the test items, configure the following parameters in the **System Settings** tab for the MIPI compliance test.

Table 6.5 Different Scenarios for Different Test Items of Group4

Test Item	D-PHY Version	High-Speed Rate	Clock Mode	Clock Lane Probing
Test 1.4.1	v1.0/1.1/1.2	≤ 1 Gbps > 1 Gbps and ≤ 1.5 Gbps > 1.5 Gbps and ≤ 2.5 Gbps	Normal	Single-ended
Test 1.4.2				
Test 1.4.3				
Test 1.4.4			Normal/ Continuous	Single-ended/ Differential
Test 1.4.5				
Test 1.4.6				Single-ended
Test 1.4.7				

Test Item	D-PHY Version	High-Speed Rate	Clock Mode	Clock Lane Probing
Test 1.4.8				
Test 1.4.9				
Test 1.4.10				
Test 1.4.11				
Test 1.4.12				
Test 1.4.13			Normal	Single-ended/Differential
Test 1.4.14				
Test 1.4.15				
Test 1.4.16				
Test 1.4.17				
Test 1.4.18	v1.1/1.2	≤ 1 Gbps > 1 Gbps and ≤ 1.5 Gbps	Normal/Continuous	Single-ended/Differential

Connection

When you select "Normal" or "Normal+Escape" from the drop-down button of **Test Mode**, you can select the following test connection methods.

- For connecting via the RTB fixture, refer to descriptions in *To Connect via the RTB Fixture*.
- For connecting the clock lane and data lane, refer to descriptions in *To Connect the Clock Lane and Data Lane*.

When you select "Continuous Data" as the clock mode, refer to connection methods in *Continuous Data Test Connection*.

6.2.5 Test Items of Group5

Group 5 HS-TX Clock-to-Data Lane Timing Requirements includes the following test items.

Test Item	Description
Test 1.5.1	HS Entry: T _{CLK-PRE} Value

Test Item	Description
Test 1.5.2	HS Exit: $T_{CLK-POST}$ Value
Test 1.5.3	HS Clock Rising Edge Alignment to First Payload Bit
Test 1.5.4	Data to Clock Skew ($T_{SKEW[TX]}$)
Test 1.5.5	Initial HS Skew Calibration Burst ($T_{SKEWCAL-SYNC}$, $T_{SKEWCAL}$)
Test 1.5.6	Period HS Skew Calibration Burst ($T_{SKEWCAL-SYNC}$, $T_{SKEWCAL}$)

Configuration Requirements

The configurations for different test items of Group5 are different. To perform the test items, configure the following parameters in the **System Settings** tab for the MIPI compliance test.

Table 6.7 Different Scenarios for Different Test Items of Group5

Test Selection	D-PHY Version	High-Speed Rate	Clock Mode	Clock Lane Probing
Test 1.5.1	v1.0/1.1/1.2	≤ 1 Gbps	Normal	Single-ended
Test 1.5.2		> 1 Gbps and ≤ 1.5 Gbps		
Test 1.5.3		> 1.5 Gbps and ≤ 2.5 Gbps	Normal/ Continuous	Single-ended/ Differential
Test 1.5.4				
Test 1.5.5	v1.2	> 1.5 Gbps and ≤ 2.5 Gbps		
Test 1.5.6				

Connection

When you select "Normal" or "Normal+Escape" from the drop-down button of **Test Mode**, you can select the following test connection methods.

- For connecting via the RTB fixture, refer to descriptions in *To Connect via the RTB Fixture*.
- For connecting the clock lane and data lane, refer to descriptions in *To Connect the Clock Lane and Data Lane*.

When you select "Continuous Data" as the clock mode, refer to connection methods in *Continuous Data Test Connection*.

6.2.6 Test Items of Eye Diagram

This test is used to measure the data signal sent from the DUT in high-speed mode. The oscilloscope captures the continuous high-speed data signal sent from the data lane, and generates the eye diagram, from which you can obtain the eye height and eye width. (This test is not the standard test item specified in the MIPI Specification.)

- HS Data Eye Height: eye height in the eye diagram.
- HS Data Eye Width: eye width in the eye diagram.

Configuration Requirements

To perform the test items of Eye Diagram Test, configure the following parameters in the **System Settings** tab for the MIPI compliance test.

- Test mode: Except Escape, all the other options are available to choose.
- Select the desired channel for Data Lane Source and Clock Lane Source based on the actual connection of the test devices.

Connection

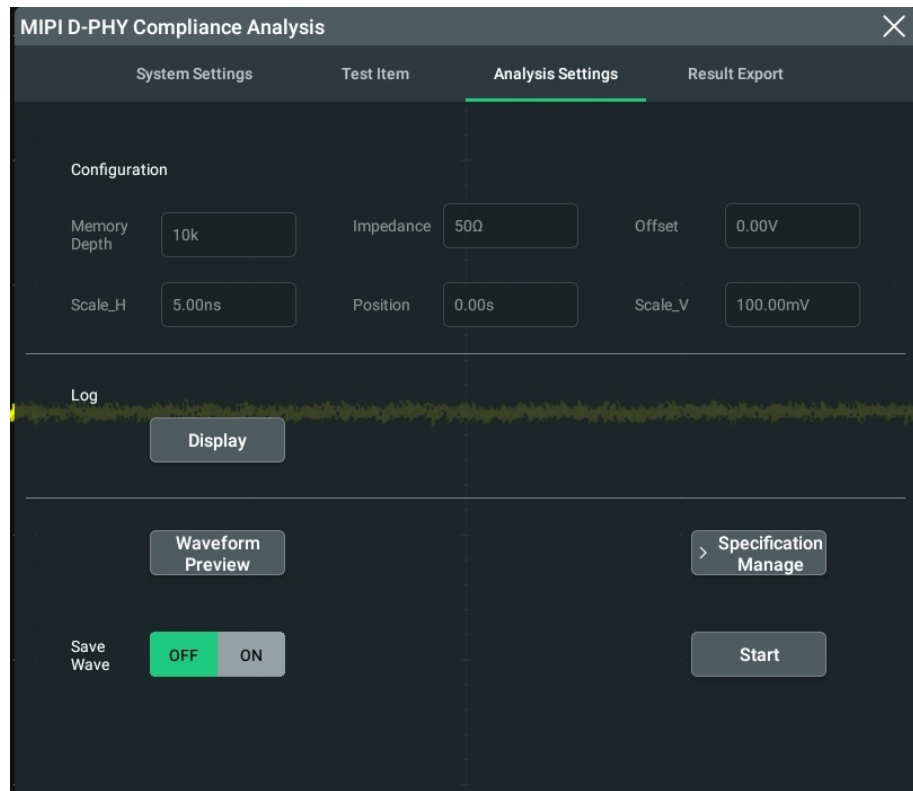
When you select "Normal" or "Normal+Escape" from the drop-down button of **Test Mode**, you can select the following test connection methods.

- For connecting via the RTB fixture, refer to descriptions in *To Connect via the RTB Fixture*.
- For connecting the clock lane and data lane, refer to descriptions in *To Connect the Clock Lane and Data Lane*.

When you select "Continuous Data" as the clock mode, refer to connection methods in *Continuous Data Test Connection*.

6.3 Analysis Settings

Click or tap **Analysis Settings** to enter the test analysis interface.



Parameter Configuration

Displays the real-time configuration of the oscilloscope and cannot be modified.

Analysis Log

Click or tap **Display**, the log interface is displayed, showing the test process log.

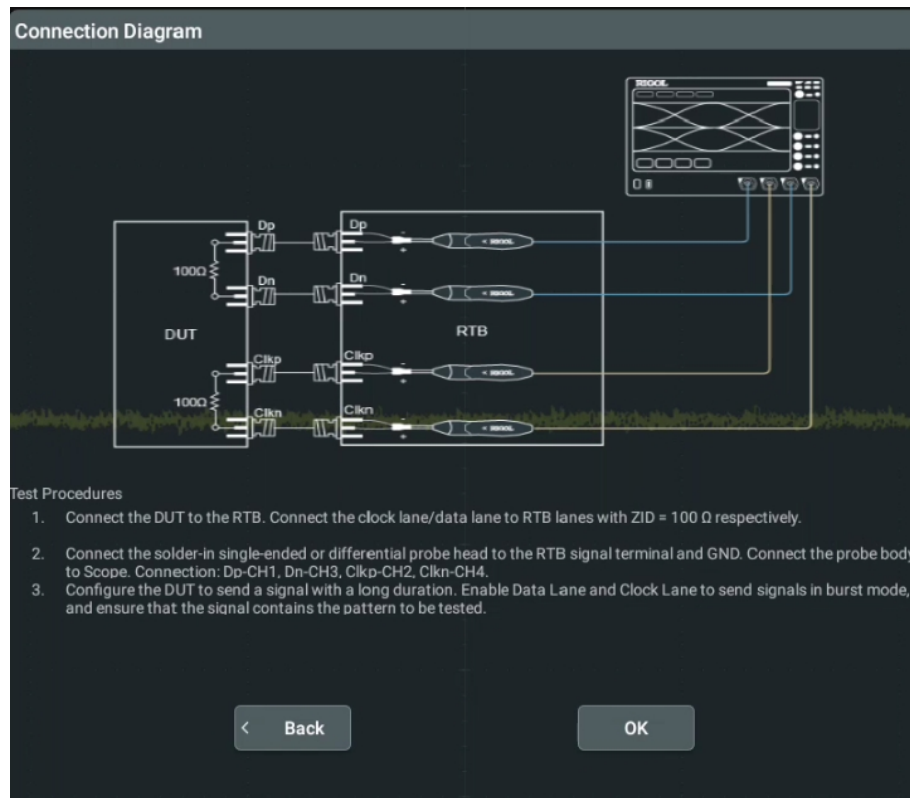
Preview and Save Waveforms

Click or tap **Waveform Preview** to preview the measured signal waveform in the waveform view. If the waveforms are proper, then start to test.

Click or tap the ON/OFF tab for **Save Wave** to enable or disable saving the waveform.

Launch the Test

After confirming that the previewed waveforms are proper, click or tap **Start** to start the test. You can connect the test devices according to the connection diagram and perform the test according to the test procedures. Click or tap **OK** to start testing the specified test item.



You are allowed to perform multiple test items at a time. During the test, if you need to adjust the connection, a prompt message will be displayed, guiding you how to operate until you completed all the test items.

If you select "Normal+Escape" for the Test Mode in the "System Settings" tab, and the test items are under both Escape mode and Normal mode, then after starting test, the oscilloscope will first prompt you with the instruction guide for the test in Escape mode. After completing the test items for Escape mode, then it prompts you on how to make tests for Normal mode. If the current DUT is available to provide these two kinds of signals, then you do not need to adjust the connection, just click or tap **Continue** to complete all the test items.

6.4 Specification Management

In the "Analysis Setting" tab, click or tap **Specification Manage** to view the parameters of the various test items of MIPI D-PHY compliance test and their conformance limits.

Specification Manage

Test Items	Min	Max	
VOH(1.1.1)	1.10V	1.30V	Default
VOL(1.1.2)	-50.00mV	50.00mV	Default
TRLP(1.1.3)		25.00ns	Default
TFLP(1.1.4)		25.00ns	Default
δV/δtSR(1.1.5)	0.00V/s	150.00mV/s	Default
TLP-PULSE-TX(1.1.6)	40.00ns		Default

< Back

Apply

Default

If you modify the value under **High-Speed Rate** in *System Settings*, the Min. and Max. values of the relevant test item parameters will change automatically. You can also modify it manually.

If the test result for different test items is within the conformance limits displayed in the **Specification Manage** interface, it indicates that the test passes. If the test result fails to meet the conformance limits, the test fails. The test result will be displayed in the test report.

In the Specification Management interface, you can set the parameter range for the specified test item. If the test result is within the conformance limit, the test passes; otherwise, the test fails.

Group1 lists the test items for the DUT low-power data lane transmitter (Data Lane LP-TX) electrical test.

Table 6.8 LP-TX Parameter Range

Test Item	Test Parameter	Description	Range	
			Min.	Max.
1.1.1	V _{OH}	Thevenin output high level	1.1 V ^[1]	1.3 V
			0.95 V ^[2]	
1.1.2	V _{OL}	Thevenin output low level	-50 mV	50 mV
1.1.3	T _{RLP}	15%-85% rise time		25 ns

Test Item	Test Parameter	Description	Range	
			Min.	Max.
1.1.4	T_{FLP}	15%-85% fall time		25 ns
1.1.5	$\delta V/\delta t_{SR}$	Slew rate@Cload = 70 pF	0	150 mV/s
1.1.6	$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	40 ns	
1.1.7	$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90 ns	

**TIP**

[1]: For DUTs supporting ≤ 1.5 Gbps

[2]: For DUTs supporting > 1.5 Gbps

Group2 lists the test items for the DUT low-power clock lane transmitter (Clock Lane LP-TX) electrical test. The parameter ranges are the same as those for the test items of Group1.

Group3 lists the test items for the DUT high-speed data lane transmitter (Data Lane HS-TX) electrical test.

Table 6.9 Data Lane HS-TX Parameter Range

Test Item	Test Parameter	Description	Range	
			Min.	Max.
1.3.1	T_{LPX}	Transitions from LP-TX to HS-TX	50 ns	
1.3.2	$T_{HS-PREPARE}$	Time to drive LP-00 before starting the HS transmission on a data lane	40 ns	85 ns
			4 UI	6 UI
1.3.3	$T_{HS-PREPARE+THS-ZERO}$	Combined time of THS-PREPARE plus the time the DUT Data Lane transmitter drives the HS-0 differential state prior to transmitting the HS Sync sequence (THS-ZERO)	(145 ns + 10*UI) ns	
1.3.4	$V_{OD(0)}$	Differential output voltage		

Test Item	Test Parameter	Description	Range	
			Min.	Max.
	$V_{OD(1)}$			
1.3.5	ΔV_{OD}	Differential voltage mismatch		14 mV
1.3.6	$V_{OHHS(DP)}$	Single-ended output high voltages at the Dp and Dn pins		360.00 mV
	$V_{OHHS(DN)}$			
1.3.7	$V_{CMTX(0)}$	Static common-mode voltages	150.00 mV	250.00 mV
	$V_{CMTX(1)}$			
1.3.8	ΔV_{CMTX}	Static common-mode voltage mismatch		5.00 mV
1.3.9	ΔV_{CMTX_LF}	Defined as a device's HS-TX Dynamic Common-Level Variations between 50 MHz and 450 MHz		25.00 mV _{peak}
1.3.10	ΔV_{CMTX_HF}	Defined as a device's HS-TX Dynamic Common-Level Variations Above 450 MHz		15.00 mV _{rms}
1.3.11	t_R	20%-80% rise time		0.30*UI ^[1]
				0.35*UI ^[2]
				0.4*UI ^[3]
1.3.12	t_F	20%-80% fall time		0.30*UI ^[1]
				0.35*UI ^[2]
				0.4*UI ^[3]
1.3.13	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns	
			4 UI	

Test Item	Test Parameter	Description	Range	
			Min.	Max.
1.3.14	T_{REOT}	A device' s LP-TX 30%-85% Rise Time, following an EoT exit from a High-Speed Data Transmission Burst		35 ns
1.3.15	T_{EOT}	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst		105 ns
				12 UI
1.3.16	$T_{HS-EXIT}$ Time that the transmitter drives LP-11 following a HS burst		100 ns	

TIP

[1]: For DUTs supporting ≤ 1.5 Gbps

[2]: For DUTs supporting > 1 Gbps and ≤ 1.5 Gbps

[3]: For DUTs supporting > 1.5 Gbps

Group4 lists the test items for the DUT high-speed clock lane transmitter (Clock Lane HS-TX) electrical test.

The parameter ranges of the test items for Test 1.4.1, Test 1.4.5 through Test 1.4.16 of Group4 are the same as those for Test 1.3.1 through Test 1.3.16.

Table 6.10 Clock Lane HS-TX Parameter Range

Test Item	Test Parameter	Description	Range	
			Min.	Max.
1.4.2	$T_{CLK-PREPARE}$	Time that the DUT Clock Lane transmitter drives LP-00 (TCLK-PREPARE) prior to driving TCLK-ZERO when entering HS mode	38 ns	95 ns
1.4.3	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	combined time of TCLK-PREPARE plus the time that the DUT Clock Lane transmitter drives the extended HS-0	300 ns	

Test Item	Test Parameter	Description	Range	
			Min.	Max.
		differential state prior to starting clock transmission (TCLK-ZERO)		
1.4.4	$V_{OD(1)}$		140 mV	270 mV
	$V_{OD(0)}$		-270 mV	-140 mV
1.4.17	UI_{INST}	A device' s instantaneous Clock Lane Unit Interval value	0 ns	12.5 ns ^[1]
1.4.18	ΔUI	A device's Unit Interval variation within a single HS burst	-10% ^[2]	10% ^[2]
			-5% ^[3]	5% ^[3]

**TIP**

[1]: Before performing Test 1.4.17 Clock Lane HS Clock Instantaneous UI (UI_{INST}), the parameter range is obtained from the DUT vendor (either directly, or via the DUT's DataSheet). You can modify the value based on your actual conditions.

[2]: For DUTs supporting ≤ 1.5 Gbps

[3]: For DUTs supporting > 1 Gbps and ≤ 1.5 Gbps

Group5: HS-TX Clock-to-Data Lane Timing Requirements**Table 6.11 HS-TX Parameter Range**

Test Item	Test Parameter	Description	Range	
			Min.	Max.
1.5.1	$T_{CLK-PRE}$	Minimum duration that the Master must transmit valid HS Clock signaling before driving any Data Lane out of LP mode.	(8*UI) ns	
1.5.2	$T_{CLK-POST}$	minimum duration that the Master must continue to transmit HS Clock signaling after the	(60 ns + 52*UI) ns	

Test Item	Test Parameter	Description	Range	
			Min.	Max.
		last Data Lane has switched to LP mode.		
1.5.4	$T_{\text{SKEW[TX]}}$	Skew between the clock and data signaling	$(0.5 - 0.15) \cdot UI$ [1]	$(0.5 + 0.15) \cdot UI$ ^[1]
			$(0.5 - 0.2) \cdot UI$ ^[2]	$(0.5 + 0.2) \cdot UI$ ^[2]
			$(0.5 - 0.2) \cdot UI$ ^[3]	$(0.5 + 0.2) \cdot UI$ ^[3]
1.5.5	$T_{\text{SKEWCAL-SYNC}}$	Initial HS Skew Calibration Burst	$(16 - 0.25) \cdot UI$	$(16 + 0.25) \cdot UI$
	T_{SKEWCAL}		$2^{12} \cdot UI$ (4096*UI)	
1.5.6	$T_{\text{SKEWCAL-SYNC}}$	Period HS Skew Calibration Burst	$(16 - 0.25) \cdot UI$	$(16 + 0.25) \cdot UI$
	T_{SKEWCAL}		$2^{12} \cdot UI$ (4096*UI)	

TIP

[1]: For DUTs supporting ≤ 1 Gbps

[2]: For DUTs supporting > 1 Gbps and ≤ 1.5 Gbps

[3]: For DUTs supporting > 1.5 Gbps

6.5 Result Report

You can view and save the test report to the local path.

Click or tap the **Report Export** tab to set the exported report information.

MIPI D-PHY Compliance Analysis

System Settings Test Item Analysis Settings **Result Export**

Save Settings

Save Format: *.html

File Name: RigolDS

File Path: Local Disk

User Info

User: RigolDS

Location: RigolDS

Temperature(°C): RigolDS

Remarks: RigolDS

Data Clear Show Save

Figure 6.2 Result Report Interface

Click or tap **Show** to view the test report. Then the web page of the test report is displayed.

Click or tap **Data Clear** to clear the history report.

Save the Report

- **Report Format**

Saves the report in "*.html" or "*.pdf" format.

- **File Name**

Inputs the file name to be saved with the pop-up numeric keypad.

- **File Path**

Click or tap the input field of **File Path**, then the disk management interface is displayed. Select the desired path where to save the report.

Set the User Information

Inputs the information of the test, and the information will be displayed in the generated test report.

**TIP**

The maximum length of the characters input with the virtual keypad shall not exceed 64. Only numbers, letter, or special symbols are required to be input.

After configuring the report information, click or tap **Save** to save the report.

7 Test Connection

Selects the specified connection method based on the actual test devices and test items. This section takes RIGOL DS80000 series oscilloscope and RIGOL PVA8700 active probe as an example to introduce the connection methods for the MIPI D-PHY compliance test solution.

When using the PVA8700 active probe to perform the test, we usually use the solder-in single-ended probe head or solder-in differential probe head to connect the probe to the DUT.

The connection methods for the Dp and Dn sources of data lane of MIPI D-PHY are as follows:

- **If solder-in differential probe head is used:**

Connect the positive polarity (+) of the probe head to Dp/Dn, and connect the negative polarity (-) of the probe head to GND.

- **If solder-in single-ended probe head (including one signal cable and one GND cable) is used, for example, *Figure 5.4*)**

connect the signal cable of the probe to Dp/Dn sources, and connect the GND cable of the probe to GND.

The connection methods for the Clkp and Clkn pins of clock lane of MIPI D-PHY are as follows:

- **For the non-continuous clock signal:** The connection methods are the same as that for the data lane, that is, single-ended probing only.
- **For the continuous clock signal:**
 - Adopts the same connection methods for the data lane.
 - Connects the positive polarity of the probe to Clkp pin of the clock lane of the DUT; connects the negative polarity of the probe to the Clkn pin of the clock lane of the DUT.

7.1 To Connect via the 50pF C_{LOAD} Test Fixture

Generally, in bare chip or PCB test scenarios, the test fixture is required to emulate RX. In the test, the 50pF C_{LOAD} test fixture is used. However, the test results are not affected by the terminal capacitor, which shall not affect the static high level and low level.

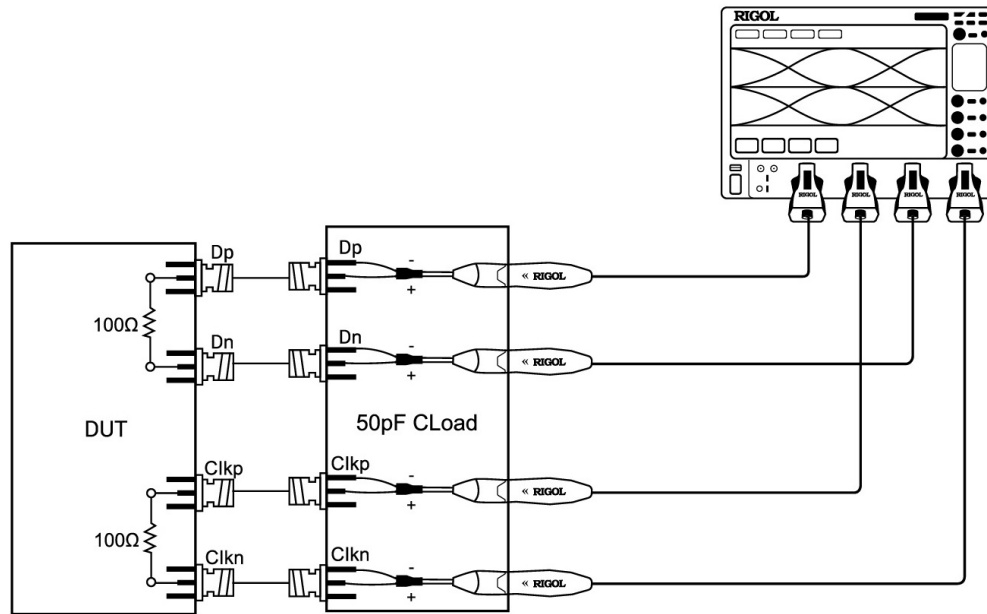


Figure 7.1 50pF C_{LOAD} Single-ended Probing for Clock Lane

When performing the following tests, you can use the 50pF C_{LOAD} fixture.

- Group 1 Data Lane LP-TX Signaling Requirements
- Group 2 Clock Lane LP-TX Signaling Requirements

7.2 To Connect via the RTB Fixture

When using the RTB (Reference Termination Board) test fixture to perform the test, we consider, by default, the differential load impedance ZID is 100 Ω.

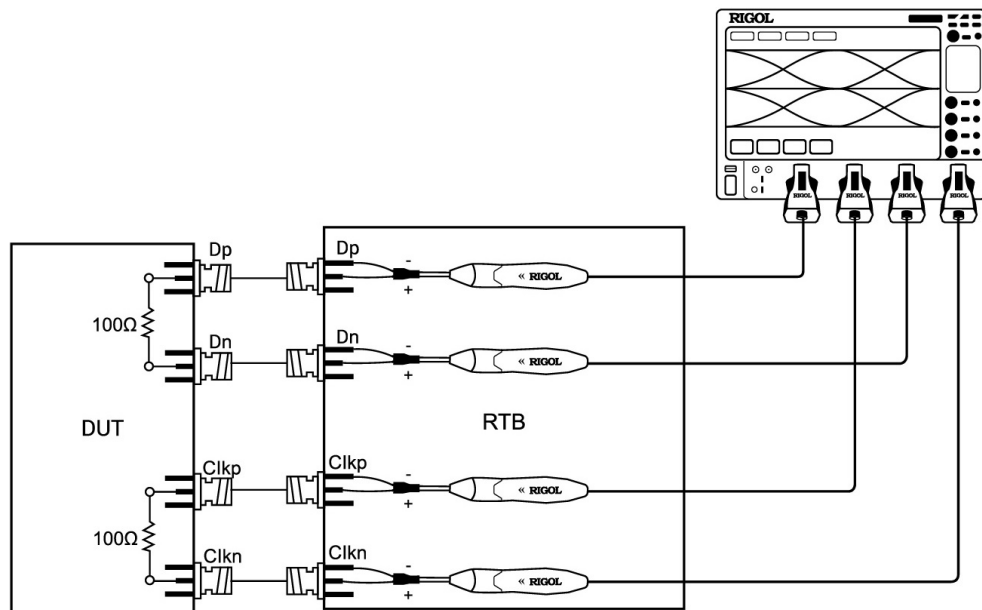


Figure 7.2 Single-ended Probing for Clock Lane on the RTB Fixture

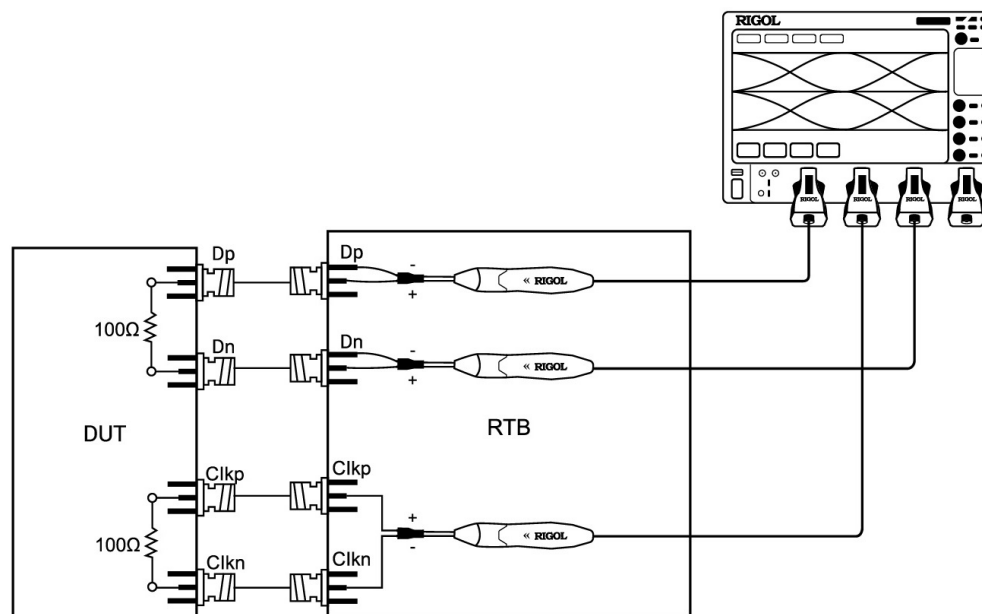


Figure 7.3 Differential Probing for Clock Lane on the RTB Fixture

Test Items Available

When performing the following tests, use the RTB fixture.

- Group 3 Data Lane HS-TX Signaling Requirements
- Group 4 Clock Lane HS-TX Signaling Requirements
- Group 5 HS-TX Clock-to-Data Lane Timing Requirements

The following table lists the test items that are only applicable for single-ended probing for clock lane.

Test Item	Description
Test 1.4.1	Clock Lane HS Entry: Clock Lane TLPX Value
Test 1.4.2	Clock Lane HS Entry: TCLK-PREPARE Value
Test 1.4.3	Clock Lane HS Entry: TCLK-PREPARE+TCLK-ZERO Value
Test 1.4.13	Clock Lane HS Exit: TCLK-TRAIL Value
Test 1.4.14	Clock Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})
Test 1.4.15	Clock Lane HS Exit: TEOT Value
Test 1.4.16	Clock Lane HS Exit: THS-EXIT Value
Test 1.4.17	Clock Lane HS Clock Instantaneous UI (UI_{INST})
Test 1.4.18	Clock Lane HS Clock Delta UI (ΔUI)
Test 1.5.1	HS Entry: $T_{CLK-PRE}$ Value
Test 1.5.2	HS Exit: $T_{CLK-POST}$ Value

7.3 To Connect the Clock Lane and Data Lane

When performing the MIPI D-PHY compliance test, no test fixture is required to emulate the receiver. You can make tests directly.

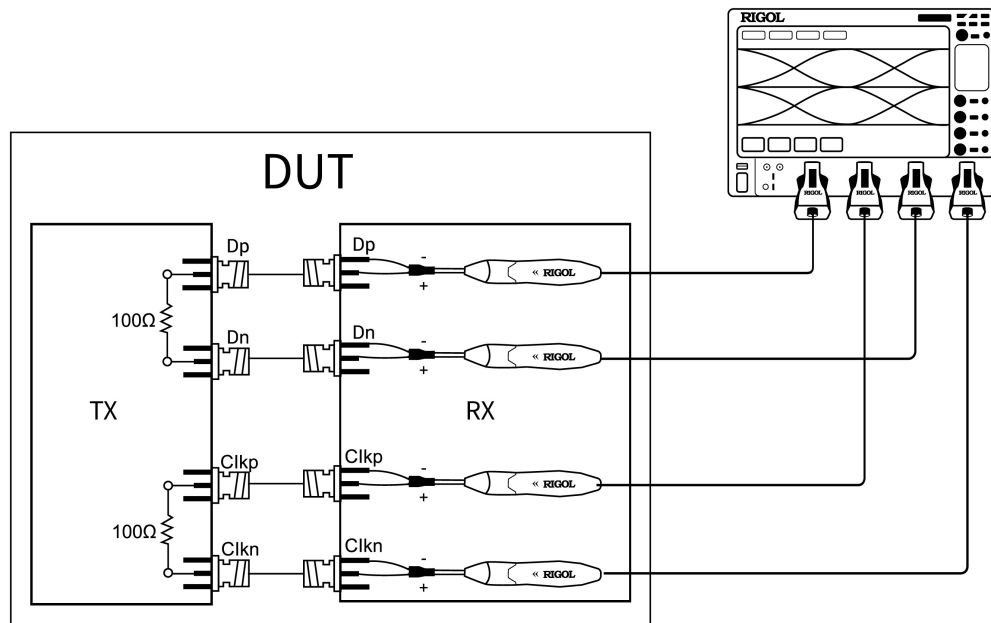


Figure 7.4 Single-ended Probing for Clock Lane and Data Lane

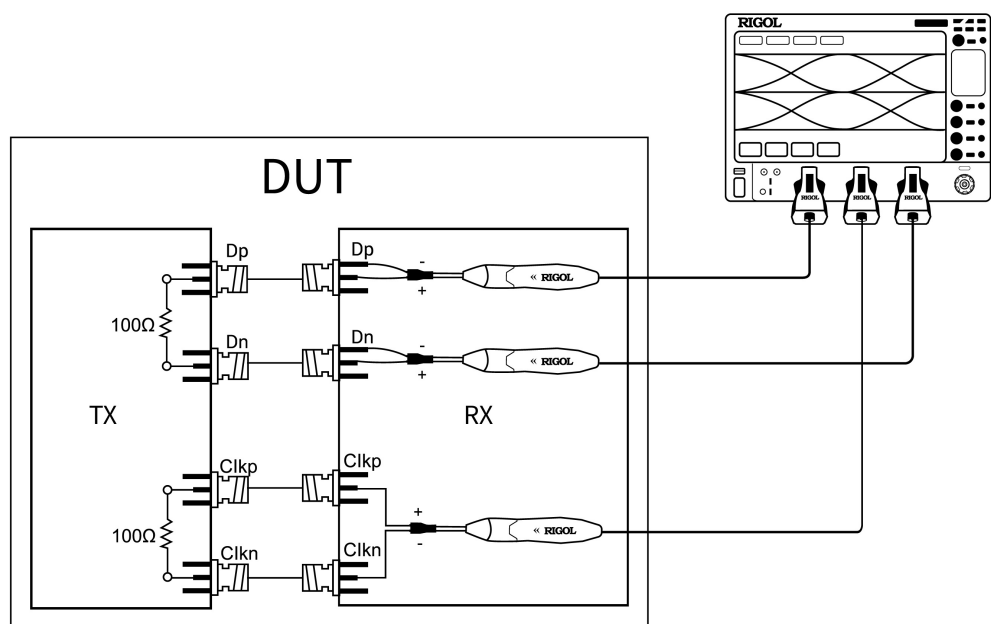


Figure 7.5 Differential Probing for Data Lane and Single-ended Probing for Clock Lane

Test Items Available

If no fixture is required, this test connection is available for test items of Group1 through Group5.

The following table lists the test items that are only applicable for single-ended clock lane probing rather than the differential probing mode.

Group	Test Item	Description
Group4	1.4.1	Clock Lane HS Entry: Clock Lane TLPX Value
	1.4.2	Clock Lane HS Entry: TCLK-PREPARE Value
	1.4.3	Clock Lane HS Entry: TCLK-PREPARE+TCLK-ZERO Value
	1.4.6	Clock Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$)
	1.4.6	Clock Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DN)}$)
	1.4.7	Clock Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}, V_{CMTX(0)}$)
	1.4.8	Clock Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$)
	1.4.9	Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($\Delta V_{CMTX(LF)}$)
	1.4.10	Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{CMTX(HF)}$)
	1.4.13	Clock Lane HS Exit: TCLK-TRAIL Value
	1.4.14	Clock Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})
	1.4.15	Clock Lane HS Exit: TEOT Value
	1.4.16	Clock Lane HS Exit: THS-EXIT Value
	1.4.17	Clock Lane HS Clock Instantaneous UI (UI_{INST})
	1.4.18	Clock Lane HS Clock Delta UI (ΔUI)
Group5	1.5.1	HS Entry: TCLK-PRE Value
	1.5.2	HS Exit: TCLK-POST Value

7.4 To Connect the Data Lane Only

When performing the MIPI D-PHY compliance test, no test fixture is required to emulate the receiver. You can make tests directly.

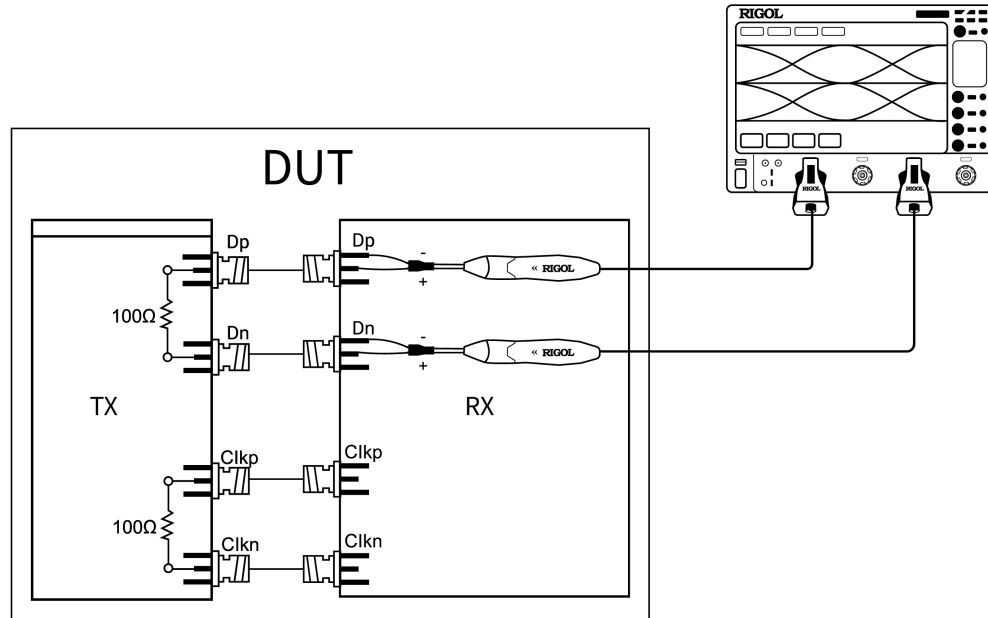


Figure 7.6 Connect Data Lane Only

Only single-end probing for data lane is supported. When performing the following tests, you can connect the data lane only.

- Group 1 Data Lane LP-TX Signaling Requirements

7.5 To Connect the Clock Lane Only

When performing the MIPI D-PHY compliance test, no test fixture is required to emulate the receiver. You can make tests directly.

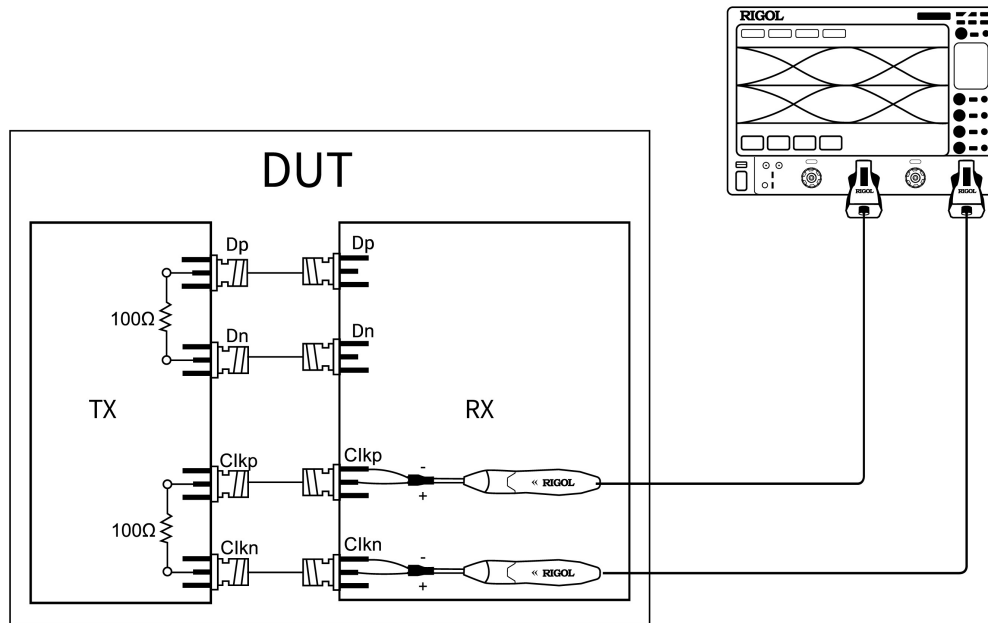


Figure 7.7 Single-ended Probing for Clock Lane

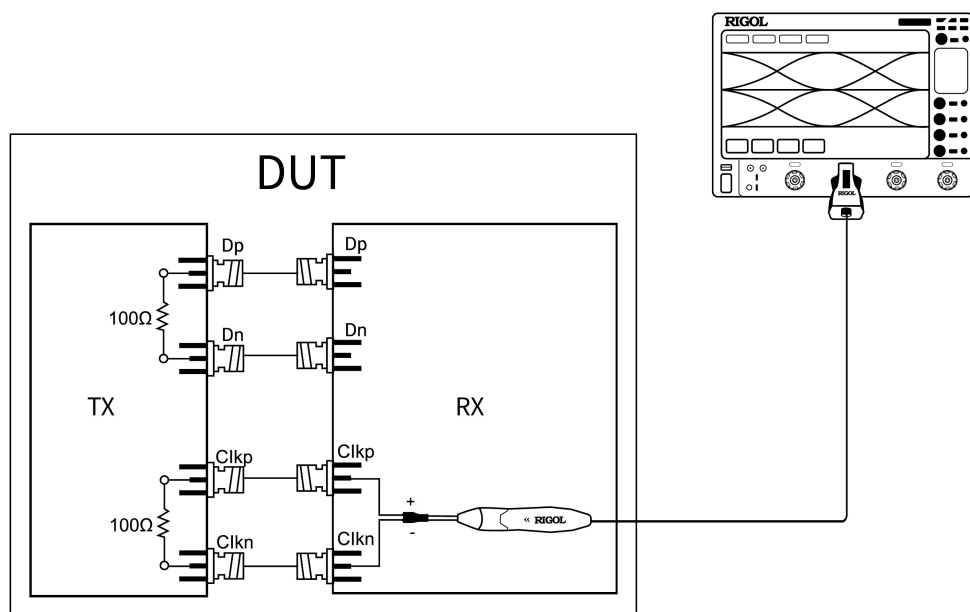


Figure 7.8 Differential Probing for Clock Lane

Test Items Available

When performing the test for the following test items of Group 4 Clock Lane HS-TX Signaling Requirements, only clock lane is required to be connected.

The following table list the test items that are only applicable for the single-ended probing for clock lane rather than the differential probing mode.

Group	Test Item	Description
Group4	1.4.1	Clock Lane HS Entry: Clock Lane TLPX Value
	1.4.2	Clock Lane HS Entry: TCLK-PREPARE Value
	1.4.3	Clock Lane HS Entry: TCLK-PREPARE+TCLK-ZERO Value
	1.4.6	Clock Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$)
	1.4.6	Clock Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DN)}$)
	1.4.7	Clock Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}, V_{CMTX(0)}$)
	1.4.8	Clock Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$)
	1.4.9	Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($\Delta V_{CMTX(LF)}$)
	1.4.10	Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{CMTX(HF)}$)
	1.4.13	Clock Lane HS Exit: TCLK-TRAIL Value
	1.4.14	Clock Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})
	1.4.15	Clock Lane HS Exit: TEOT Value
	1.4.16	Clock Lane HS Exit: THS-EXIT Value
	1.4.17	Clock Lane HS Clock Instantaneous UI (UI_{INST})
	1.4.18	Clock Lane HS Clock Delta UI (ΔUI)

7.6 Continuous Data Test Connection

The connection for Continuous Data Test is only available for the test items when the test mode in *System Settings* is set to "Continuous Data". In this mode, the clock and data lanes of the DUT send continuous high-speed clock and data signals. At this time, "Continuous" is only available to choose under "Clock Mode".

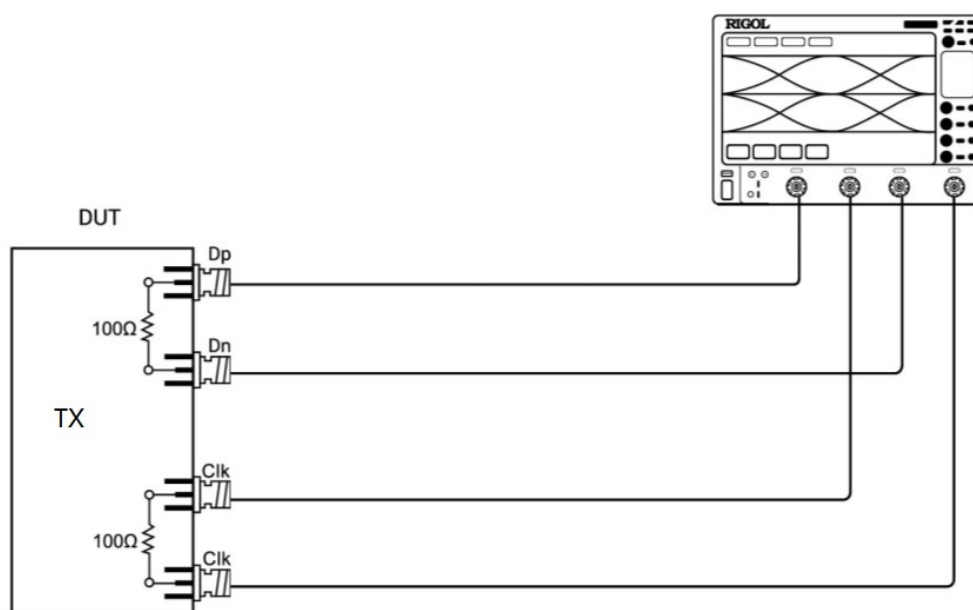


Figure 7.9 Continuous Data Test Connection

As shown in the figure above, the DUT is the transmitter. The receiver load is the analog channel with 50 Ω input impedance. The analog channel of the DS80000 series oscilloscope is an SMA connector. Please select a proper cable based on the actual interface type of the DUT.

Test Items for Continuous Data Test

The following table lists the test items for Continuous Data Test.

Group	Test Item	Description
Group3	Test 1.3.4	Data Lane HS-TX Differential Voltages ($V_{OD(0)}$, $V_{OD(1)}$)
	Test 1.3.5	Data Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})
	Test 1.3.6	Data Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$)
	Test 1.3.6	Data Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DN)}$)
	Test 1.3.7	Data Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}$, $V_{CMTX(0)}$)
	Test 1.3.8	Data Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{CMTX(1,0)}$)

Group	Test Item	Description
	Test 1.3.9	Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($\Delta V_{\text{CMTX(LF)}}$)
	Test 1.3.10	Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{\text{CMTX(HF)}}$)
	Test 1.3.11	Data Lane HS-TX 20%-80% Rise Time (t_R)
	Test 1.3.12	Data Lane HS-TX 80%-20% Fall Time (t_F)
Group4	Test 1.4.4	Clock Lane HS-TX Differential Voltages ($V_{\text{OD(0)}}, V_{\text{OD(1)}}$)
	Test 1.4.5	Clock Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})
	1.4.6	Clock Lane HS-TX Single-Ended Output High Voltages ($V_{\text{OHHS(DP)}}$)
	1.4.6	Clock Lane HS-TX Single-Ended Output High Voltages ($V_{\text{OHHS(DN)}}$)
	1.4.7	Clock Lane HS-TX Static Common-Mode Voltages ($V_{\text{CMTX(1)}}, V_{\text{CMTX(0)}}$)
	1.4.8	Clock Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{\text{CMTX(1,0)}}$)
	1.4.9	Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($\Delta V_{\text{CMTX(LF)}}$)
	1.4.10	Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{\text{CMTX(HF)}}$)
	Test 1.4.11	Clock Lane HS-TX 20%-80% Rise Time (t_R)
	Test 1.4.12	Clock Lane HS-TX 80%-20% Fall Time (t_F)
Group5	1.5.4	Data to Clock Skew (TSKEW[TX])

8 Group 1 Data Lane LP-TX Signaling Requirements

This group of tests verify various requirements specific to Data Lane LP signaling.

This group is available when you select "Normal+Escape" as the test mode. Set the DUT to send the ULPS Entry waveform sequence or Escape Exit waveform sequence, then perform the test on the specified waveforms.

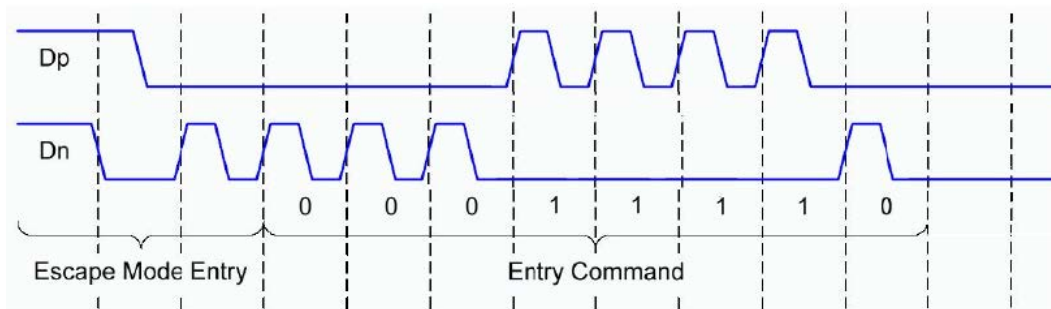


Figure 8.1 ULPS Entry Waveform Sequence

- Escape Mode Entry: sends LP-11 -> 10 -> 00 -> 01 -> 00 sequence, then data lane enter Escape mode.
- Entry Command: After the data lane enters Escape mode. The transmitter (TX) sends the Entry Command (00011110), indicating that it enters ULPS mode.

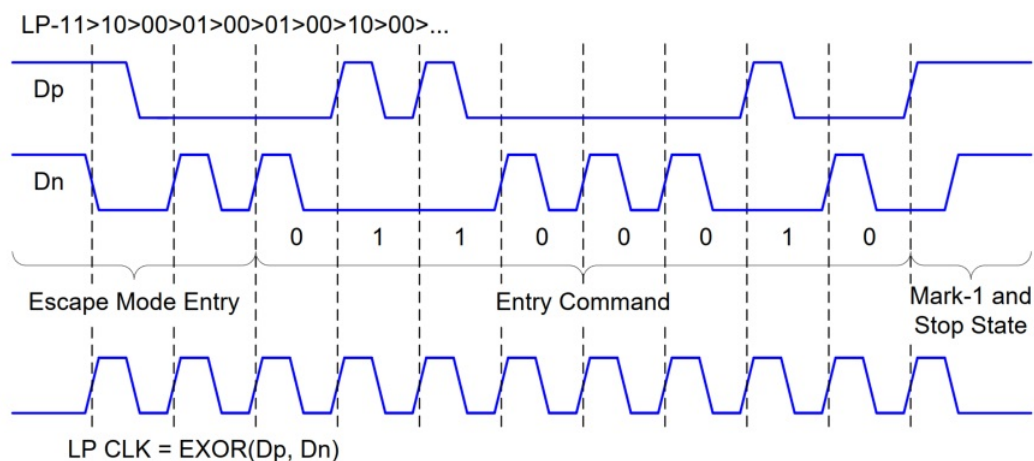


Figure 8.2 Escape Exit Waveform Sequence

- Escape Mode Entry: send LP-11 -> 10 -> 00 -> 01 -> 00 sequence, then data lane enter Escape mode.

- Entry Command: After the data lane enters Escape mode. The transmitter (TX) sends the Entry Command (01100010), indicating sending the Reset-Trigger request.
- Mark-1 and Stop State: data lane returns from LP-00 (Bridge state) to LP-11 (Stop state), and the Escape mode terminates.

**NOTE**

This group of tests are generally performed on the master DUT, and they are not available for slave DUT.

8.1 Group1 Test Procedures

Refer to *To Connect via the 50pF CLOAD Test Fixture* and *To Connect the Data Lane Only* to connect the oscilloscope, probe, 50 pF C_{LOAD} test fixture, and the DUT.

Open the MIPI compliance test interface, as shown in *Figure 6.1*.

1. Click or tap the "System Settings" tab to configure the test.
 - Select the desired D-PHY version and High-Speed Rate according to the actual situation of the DUT.
 - Select "Escape" or "Normal+Escape" from the drop-down button of "Test Mode".
 - Based on the test device connection, select "CH1" as the D+ source and "CH3" as the D- source of the Data Lane.
2. Click or tap the "Test Item" tab, and check the checkbox of Group1 and all of test items under it.
3. Adjust and observe the specified signal sequence sent from the data lane of the DUT.
4. Click or tap the "Analysis Settings" tab. Click or tap **Start** to perform the test according to its instructions.
5. Click or tap the "Result Export" tab to configure the result export, save and export the report.

Analyze the test report, and observe the test results for each test item.

6. If the DUT has multiple data lanes, repeat the test procedures mentioned above to complete the test for all the data lanes.

8.2 Test 1.1.1 Data Lane LP-TX Thevenin Output High Level Voltage (V_{OH})

This test verifies whether the measured V_{OH} value for the test signal is within the conformance limit.

V_{OH} is the Thevenin output high-level voltage V_{Dp} and V_{Dn} in the high-level state. This is the voltage at an unloaded pad pin Dp and Dn of the data lane in the LP transmit mode (LP-TX). The measured voltage V_{Dp} of the Dp pin and the measured voltage V_{Dn} of the Dn pin shall meet the requirement of V_{OH} .

Test Procedures

Configure the DUT to send the ULPS Entry waveform sequence on the data lane, as shown in [Figure 8.1](#).

Refer to [Group1 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Nom.	Max.
V_{OH}	≤ 1.5 Gbps	1.1 V	1.2 V	1.3 V
	> 1.5 Gbps	0.95 V		1.3 V

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 21.

8.3 Test 1.1.2 Data Lane LP-TX Thevenin Output Low Level Voltage (V_{OL})

This test verifies whether the measured V_{OL} value for the test signal is within the conformance limit.

V_{OL} is the Thevenin output low-level voltage V_{Dp} and V_{Dn} in the low-level state, when the pad pin Dp and Dn of the data lane are not loaded for the data lane of the DUT in low-power transmitter state (LP-TX). The measured voltage V_{Dp} of the Dp pin and the measured voltage V_{Dn} of the Dn pin shall meet the requirement of V_{OL} .

Test Procedures

Configure the DUT to send the ULPS Entry waveform sequence on the data lane, as shown in [Figure 8.1](#).

Refer to [Group1 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Nom.	Max.
V_{OL}	-	-50 mV		50 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 21.

8.4 Test 1.1.3 Data Lane LP-TX 15%-85% Rise Time (T_{RLP})

This test verifies whether the 15%-85% Rise Time (T_{RLP}) value of the DUT's data lane in LP-TX state is within the conformance limit.

This test uses the output voltage V_{OH} and V_{OL} obtained from [Test 1.1.1](#) and [Test 1.1.2](#) as the reference to calculate the 15%-85% rise time (T_{RLP}).

Test Procedures

Configure the DUT to send the ULPS Entry waveform sequence on the data lane, as shown in [Figure 8.1](#).

Refer to [Group1 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Nom.	Max.
T_{RLP}	≤ 1.5 Gbps			25 ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 22.

8.5 Test 1.1.4 Data Lane LP-TX 15%-85% Fall Time (T_{FLP})

This test verifies whether the 15%-85% Fall Time (T_{FLP}) value of the DUT's data lane in LP-TX state is within the conformance limit.

This test uses the output voltage V_{OH} and V_{OL} obtained from [Test 1.1.1](#) and [Test 1.1.2](#) as the reference to calculate the 15%-85% fall time (T_{FLP}).

Test Procedures

Configure the DUT to send the ULPS Entry waveform sequence on the data lane, as shown in [Figure 8.1](#).

Refer to [Group1 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Nom.	Max.
T_{FLP}	≤ 1.5 Gbps			25 ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 22.

8.6 Test 1.1.5 Data Lane LP-TX Slew Rate vs. CLOAD ($\delta V/\delta t_{SR}$)

This test verifies whether the Slew Rate ($\delta V/\delta t_{SR}$) value of the DUT's data lane in LP-TX state is within the conformance limit.

- The slew rate ($\delta V/\delta t_{SR}$) is the derivative of the LP transmitter output signal voltage over time. It is used to measure the LP transmitter output signal transitions.
- The slew rate ($\delta V/\delta t_{SR}$) is related to the capacitive load. This test adopts the 50 50pF C_{LOAD} .

Refer to [Test 1.1.3](#) and [Test 1.1.4](#) to obtain the value of the rising and falling edge of the waveform sequence sent on the data lane to get the slew rate.

Test Procedures

Configure the DUT to send the ULPS Entry waveform sequence on the data lane, as shown in [Figure 8.1](#).

Refer to [Group1 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

	DUT Rate	Edge Type	Amplitude Range	Min.	Max.
$\delta V/\delta t_{SR}$	≤ 1.5 Gbps	Falling Edge	Entire Signal Transition/Edge		150 mV/ns
			400 mV to 930 mV	30 mV/ns	
		Rising Edge	Entire Signal Transition/Edge		
			400 mV to 700 mV	30 mV/ns	
			700 mV to 930 mV	0 mV/ns	
		> 1.5 Gbps	Falling Edge	Entire Signal Transition/Edge	
	400 mV to 790 mV			25 mV/ns	
	Rising Edge		Entire Signal Transition/Edge		
			400 mV to 550 mV	25 mV/ns	
			550 mV to 790 mV	0 mV/ns	

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 22.

8.7 Test 1.1.6 Data Lane LP-TX Pulse Width of Exclusive-OR Clock ($T_{LP-PULSE-TX}$)

This test verifies whether the pulse width ($T_{LP-PULSE-TX}$) value of the DUT's data lane in LP-TX state is within the conformance limit.

Configures the DUT data lane to send the waveform sequence shown in [Figure 8.2](#). In the figure, the waveform sequence at the bottom is the graphical example of the XOR operation for the signal V_{Dp} and V_{Dn} . $LP\ CLK = EXOR(D_p, D_n)$. $T_{LP-PULSE-TX}$ is the pulse width of the clock signal.

Refer to [Test 1.1.1](#) and [Test 1.1.2](#) to perform measurements on V_{Dp} and V_{Dn} signal.

Test Procedures

Configures the DUT to send the waveform sequence shown in [Figure 8.2](#). Refer to [Group1 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$T_{LP-PULSE-TX}$	≤ 1.5 Gbps	40 ns	

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 22.

8.8 Test 1.1.7 Data Lane LP-TX Period of Exclusive-OR Clock ($T_{LP-PER-TX}$)

This test verifies whether the period ($T_{LP-PER-TX}$) value of the DUT's data lane LP transmitter XOR clock is within the conformance limit.

Configures the DUT data lane to send the waveform sequence shown in [Figure 8.2](#). In the figure, the waveform sequence at the bottom is the graphical example of the XOR operation for the signal V_{Dp} and V_{Dn} . $LP\ CLK = EXOR(D_p, D_n)$. $T_{LP-PER-TX}$ is the period of the DUT LP-TX XOR clock.

Refer to [Test 1.1.1](#) and [Test 1.1.2](#) to perform measurements on V_{Dp} and V_{Dn} signal.

Test Procedures

Configures the DUT to send the waveform sequence shown in [Figure 8.2](#). Refer to [Group1 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Edge Type	Min.	Max.
$T_{LP-PER-TX}$	≤ 1.5 Gbps	Rising Edge	90 ns	
		Falling Edge	90 ns	

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 22 and Table 25.

9 Group 2 Clock Lane LP-TX Signaling Requirements

This group of tests verify various requirements specific to Clock Lane LP signaling.

This group of tests are required to configure the clock lane of the DUT to send ULPS Entry sequence and ULPS Exit sequence.

- ULPS Entry sequence: LP-11>10>00
- ULPS Exit sequence: LP-00>10>11 or Mark-1/Stop



NOTE

This group of tests are generally performed on the master DUT, and they are not available for slave DUT.

9.1 Group2 Test Procedures

Refer to *To Connect via the 50pF CLOAD Test Fixture* and *To Connect the Clock Lane Only* to connect the oscilloscope, probe, 50 pF C_{LOAD} test fixture, and the DUT.

Open the MIPI compliance test interface, as shown in *Figure 6.1*.

1. Click or tap the "System Settings" tab to configure the test.
 - Select the desired D-PHY version and High-Speed Rate according to the actual situation of the DUT.
 - Select "Escape" or "Normal+Escape" from the drop-down button of "Test Mode".
 - Click or tap the drop-down button of **Clock Mode** to select "Normal".
 - Click or tap the drop-down button of **Clock Lane Probe** to select "Single-ended".
 - Based on the test device connection, select "CH2" as the D+ source and "CH4" as the D- source of the Clock Lane.
2. Click or tap the "Test Item" tab, and check the checkbox of Group2 and all of test items under it.
3. Adjust and observe the specified signal sequence sent from the clock lane of the DUT.

4. Click or tap the "Analysis Settings" tab. Click or tap **Start** to perform the test according to its instructions.
5. Click or tap the "Result Export" tab to configure the result export, save and export the report.

Analyze the test report, and observe the test results for each test item.

9.2 Test 1.2.1 Clock Lane LP-TX Thevenin Output High Level Voltage (V_{OH})

This test verifies whether the measured V_{OH} value for the test signal is within the conformance limit.

The test methods are similar with those for the test items of [Test-1.1.1](#). This test tests the voltage at an unloaded pad pin (Clkp and Clkn) of the clock lane in the high-level state for the output signal V_{Dp} and V_{Dn} to obtain the V_{OH} value.

Test Procedures

Configure the DUT clock lane to send the typical ULPS Entry waveform sequence to perform this test according to descriptions in [Group2 Test Procedures](#).

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Nom.	Max.
V_{OH}	≤ 1.5 Gbps	1.1 V	1.2 V	1.3 V
	> 1.5 Gbps	0.95 V		1.3 V

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 21.

9.3 Test 1.2.2 Clock Lane LP-TX Thevenin Output Low Level Voltage (V_{OL})

This test verifies whether the measured V_{OL} value for the test signal is within the conformance limit.

The test methods are similar with those for the test items of [Test 1.1.2](#). This test tests the voltage at an unloaded pad pin (Clkp and Clkn) of the clock lane in the low-level state for the output signal V_{Dp} and V_{Dn} in the low-level state. This is the voltage V_{OL} value.

Requirements

Test Procedures

Configure the DUT clock lane to send the typical ULPS Entry waveform sequence to perform this test according to descriptions in *Group2 Test Procedures*.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Nom.	Max.
V_{OL}		-50 mV		50 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 21.

9.4 Test 1.2.3 Clock Lane LP-TX 15%-85% Rise Time (T_{RLP})

This test verifies whether the 15%-85% Rise Time (T_{RLP}) value of the DUT's clock lane LP transmitter is within the conformance limit.

As the ULPS Entry sequence of the clock lane is different from that of the data lane, which excludes any rising edge. Perform the test on the rising edge of the ULPS Exit sequence (Mark-1/Stop or LP-00>10>11) waveform of the clock lane.

This test uses the output voltage V_{OH} and V_{OL} obtained from *Test 1.2.1* and *Test 1.2.2* as the reference to calculate the 15%-85% rise time (T_{RLP}).

Test Procedures

Configure the DUT clock lane to send the typical ULPS Exit waveform sequence (Mark-1/Stop) to perform this test according to descriptions in *Group2 Test Procedures*.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Nom.	Max.
T_{RLP}	≤ 1.5 Gbps			25 ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 22.

9.5 Test 1.2.4 Clock Lane LP-TX 15%-85% Fall Time (T_{FLP})

This test verifies whether the 15%-85% Fall Time (T_{FLP}) value of the DUT's clock lane LP transmitter is within the conformance limit.

This test uses the output voltage V_{OH} and V_{OL} obtained from [Test 1.2.1](#) and [Test 1.2.2](#) as the reference to calculate the 15%-85% fall time (T_{FLP}).

Test Procedures

Configure the DUT clock lane to send the typical ULPS Entry waveform sequence to perform this test according to descriptions in [Group2 Test Procedures](#).

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Nom.	Max.
T_{FLP}	≤ 1.5 Gbps			25 ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 22.

9.6 Test 1.2.5 Clock Lane LP-TX Slew Rate vs. CLOAD ($\delta V/\delta t_{SR}$)

This test verifies whether the Slew Rate ($\delta V/\delta t_{SR}$) value of the DUT's clock lane in LP-TX state is within the conformance limit.

- The slew rate ($\delta V/\delta t_{SR}$) is the derivative of the LP transmitter output signal voltage over time. It is used to measure the LP transmitter output signal transitions.
- The slew rate ($\delta V/\delta t_{SR}$) is related to the capacitive load. This test adopts the 50 pF C_{LOAD} .

Refer to [Test 1.2.3](#) and [Test 1.2.4](#) to obtain the value of the rising and falling edge of the waveform sequence sent on the clock lane to get the slew rate.

Test Procedures

Configure the DUT clock lane to send the typical ULPS Entry waveform sequence to perform this test according to descriptions in [Group2 Test Procedures](#).

Pass Conditions

The test results shall meet the following conditions:

Requirements

Parameter	DUT Rate	Edge Type	Amplitude Range	Min.	Max.
$\delta V/\delta t_{SR}$	≤ 1.5 Gbps	Falling Edge	Entire Signal Transition/Edge		150 mV/ns
			400 to 930 mV	30 mV/ns	
		Rising Edge	Entire Signal Transition/Edge		
			400 mV to 700 mV	30 mV/ns	
			700 mV to 930 mV	0 mV/ns	
		> 1.5 Gbps	Falling Edge	Entire Signal Transition/Edge	
	400 mV to 790 mV			25 mV/ns	
	Rising Edge		Entire Signal Transition/Edge		
			400 mV to 550 mV	25 mV/ns	
			550 mV to 790 mV	0 mV/ns	

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.2, Table 22.

10 Group 3 Data Lane HS-TX Signaling Requirements

This section introduces the test methods for the test items of Group3 when you select "Normal" or "Normal+Escape" as the test mode in *System Settings*. If you select "Continuous Data" as the clock mode, refer to descriptions in *Continuous Data Test Mode*.

This group of tests verify various TX requirements specific to Data Lane HS burst signaling.

This group of tests configure the oscilloscope to capture the HS burst waveforms sent from the DUT, which includes the LP exist/entry sequences occurring before and after the burst sequence. The sequence starts from and ends at LP-11, as shown in the figure below.

For this group of tests, configure the data lane of the DUT to enter the high-speed burst data transmission state, as shown in the figure below.

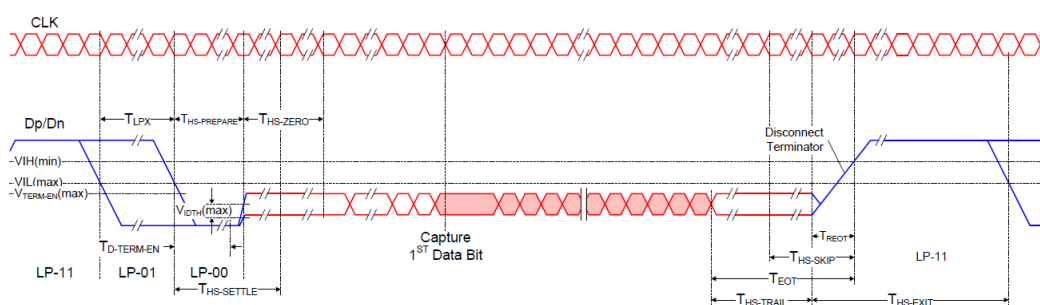


Figure 10.1 High-Speed Data Burst Sequence

The sequence sent from the data lane starts from LP-11 and ends with LP-11. It includes LP exit/entry sequences occurring before and after the burst sequence. The sequence of events during the transmission of a data burst is as follows: LP-11(Stop) -> LP-01(HS-Rqst) -> LP-00(Bridge) -> HS-0, then comes the Sync word (HS-00011101). After that, differential data are sent continuously until all the data are sent. At the end of a data burst, the data lane exists the high-speed mode and enters the stop state.

The continuous clock signal are sent from the clock lane. During the transmission, the clock lane will not switch to LP state, remaining the clock rate and slew rate unchanged.

NOTE

This group of tests are generally performed on the master DUT, and they are not available for slave DUT.



10.1 Group3 Test Procedures

Connect the Device

Connect the oscilloscope, active probe, RTB test fixture, and DUT. For detailed connection methods, refer to *To Connect via the RTB Fixture* or *To Connect the Clock Lane and Data Lane*.

Configure the DUT

Configure the DUT to send high-speed burst signal on the data lane, as shown in *Figure 10.1*.

Configure the oscilloscope to perform the MIPI compliance test

Open the MIPI compliance test interface, as shown in *Figure 6.1*.

1. Click or tap the "System Settings" tab to configure the test.
 - Select the desired D-PHY version and High-Speed Rate according to the actual situation of the DUT.
 - Select "Escape" or "Normal+Escape" from the drop-down button of "Test Mode".
 - Based on the test device connection, select "CH1" as the D+ source and "CH3" as the D- source of the Data Lane. Select "CH2" as the D+ source and "CH4" as the D- source of the Clock Lane.
2. Click or tap the "Test Item" tab, and check the checkbox of Group3 and all of test items under it.
3. Observe the HS burst waveform sequence captured by the oscilloscope on the data lane.
4. Click or tap the "Analysis Settings" tab. Click or tap **Start** to perform the test according to its instructions.
5. Click or tap the "Result Export" tab to configure the result export, save and export the report.

Analyze the test report, and observe the test results for each test item.
6. If the DUT has multiple data lanes, repeat the test procedures mentioned above to complete the test for all the data lanes.

10.2 Test 1.3.1 Data Lane HS Entry: Data Lane T_{LPX} Value

This test verifies whether the last LP-01's duration (T_{LPX}) value prior to HS Data burst is within the conformance limit.

As shown in [Figure 10.1](#), the duration of the last LP-01 state that occurs immediately before an HS burst sequence. This duration is defined as T_{LPX} . The state will be measured starting at the time where the V_{DP} falling edge crosses below the maximum low-level LP threshold ($V_{IL, MAX}$ (550 mV), and ending at the time where the V_{DN} falling edge crosses below the same $V_{IL, MAX}$ threshold.

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions: $T_{LPX} \geq 50$ ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.2, Table 14.

Test Result Reference

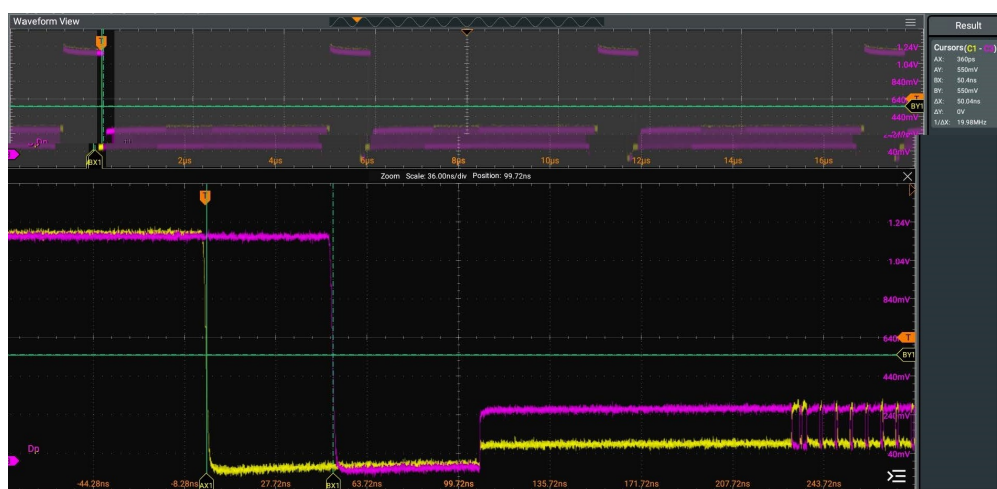


Figure 10.2 Test 1.3.1 Test Waveform and Result

10.3 Test 1.3.2 Data Lane HS Entry: $T_{HS-PREPARE}$ Value

This test verifies whether the last LP-00's duration ($T_{HS-PREPARE}$) value prior to HS Data burst is within the conformance limit, as shown in [Figure 10.1](#).

Before switching the data lane into HS burst sequence mode (which occurs at the start of the $T_{HS-ZERO}$ interval), the D-PHY Specification requires the minimum time interval that a device must transmit the final LP-00 state. This interval is defined as

Requirements

$T_{HS-PREPARE}$. The $T_{HS-PREPARE}$ value is measured starting at the time where the data lane V_{Dn} signal crosses below $V_{IL, MAX}$ (550 mV), and ends at the beginning of the extended THS-ZERO HS differential state, at the point where the differential waveform crosses above the minimum valid HS-0 differential threshold (-70 mV).

As shown in [Figure 10.1](#), before switching the data lane into HS burst sequence mode (which occurs at the start of the $T_{HS-ZERO}$ interval), the D-PHY Specification requires the minimum time interval that a device must transmit the final LP-00 state. This interval is defined as $T_{HS-PREPARE}$. The state will be measured starting at the time where the V_{Dn} signal crosses below $V_{IL, MAX}$ (550 mV), and ends at the beginning of the extended THS-ZERO HS differential state, at the point where the differential waveform crosses above the minimum valid HS-0 differential threshold (-70 mV).

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$T_{HS-PREPARE}$		40 ns + 4*UI	85 ns + 6*UI

Wherein, UI is the nominal HS Unit Interval for the DUT, see [Test 1.4.17](#).

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.14.2, Table 14.

Test Result Reference

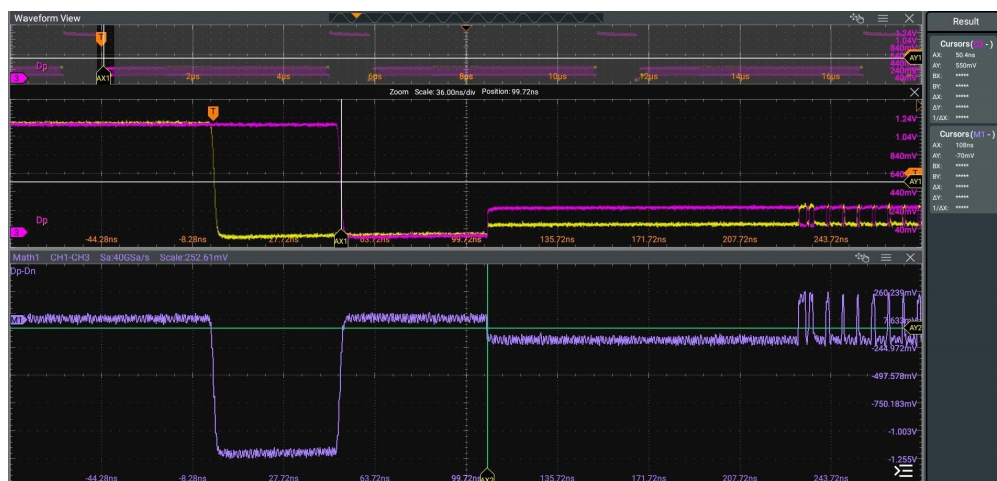


Figure 10.3 Test 1.3.2 Test Waveform and Result

10.4 Test 1.3.3 Data Lane HS Entry: $T_{\text{HS-PREPARE}} + T_{\text{HS-ZERO}}$ Value

This test verifies that the combined time of $T_{\text{HS-PREPARE}}$ plus $T_{\text{HS-ZERO}}$ is greater than the minimum required duration.

- For the definition of $T_{\text{HS-PREPARE}}$, refer to [Test 1.3.2](#).
- $T_{\text{HS-ZERO}}$ is the minimum duration that a device must drive the extended data HS-0 differential state ($V_{\text{Dp}} < V_{\text{Dn}}$) prior to starting HS differential data transmission.

As shown in [Figure 10.1](#), the ($T_{\text{HS-PREPARE}} + T_{\text{HS-ZERO}}$) interval begins at the time where the data lane V_{Dn} signal crosses below $V_{\text{IL, MAX}}$ (550 mV), and ends at the end of the extended $T_{\text{HS-ZERO}}$ HS-0 differential state.

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$T_{\text{HS-PREPARE}} + T_{\text{HS-ZERO}}$		145 ns + 10*UI	

Wherein, UI is the nominal HS Unit Interval for the DUT, see [Test 1.4.17](#).

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.14.2, Table 14.

Test Result Reference



Figure 10.4

10.5 Test 1.3.4 Data Lane HS-TX Differential Voltages ($V_{OD(0)}$, $V_{OD(1)}$.)

This test verifies whether the differential voltages ($V_{OD(0)}$ and $V_{OD(1)}$) of the DUT data lane HS transmitter are within the conformance limit.

The differential output voltage V_{OD} is defined as the difference of the voltages V_{Dp} and V_{Dn} at the Dp and Dn pins, as shown in the figure below.

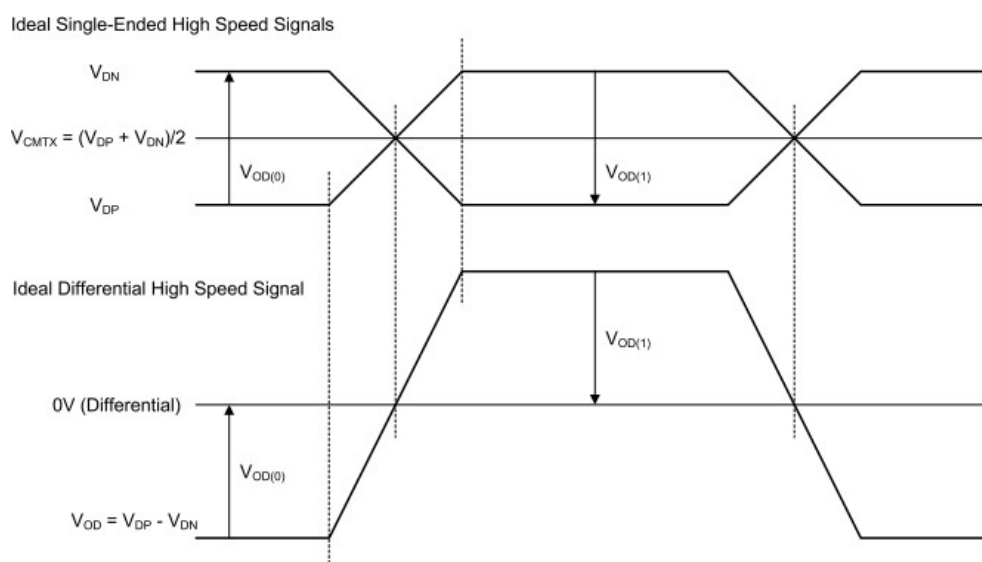


Figure 10.5 Ideal Single-ended and Differential High Speed Signal

$$V_{OD} = V_{Dp} - V_{Dn}$$

- $V_{OD(0)}$: indicates a device's HS-TX differential voltage level for the HS-0 state ($V_{Dp} < V_{Dn}$).
- $V_{OD(1)}$: indicates a device's HS-TX differential voltage level for the HS-1 state ($V_{Dp} > V_{Dn}$).

Test Procedures

Refer to *Group3 Test Procedures* to perform the test.

If the DUT has the load impedance, connect the data lane to the $Z_{ID} = 125\ \Omega$ and $Z_{ID} = 80\ \Omega$ lane of the RTB, then repeat the above test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$V_{OD(1)}$		140mV	270mV
$V_{OD(0)}$		-270mV	-140mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

Test Result Reference

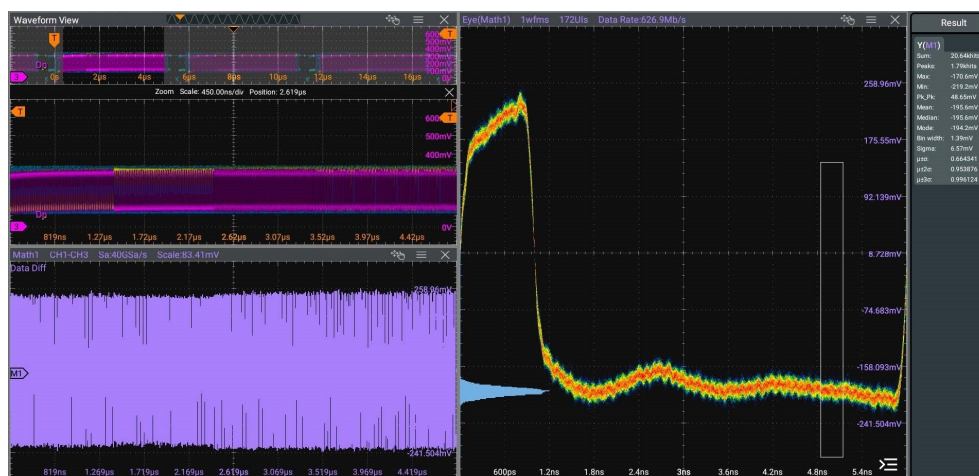
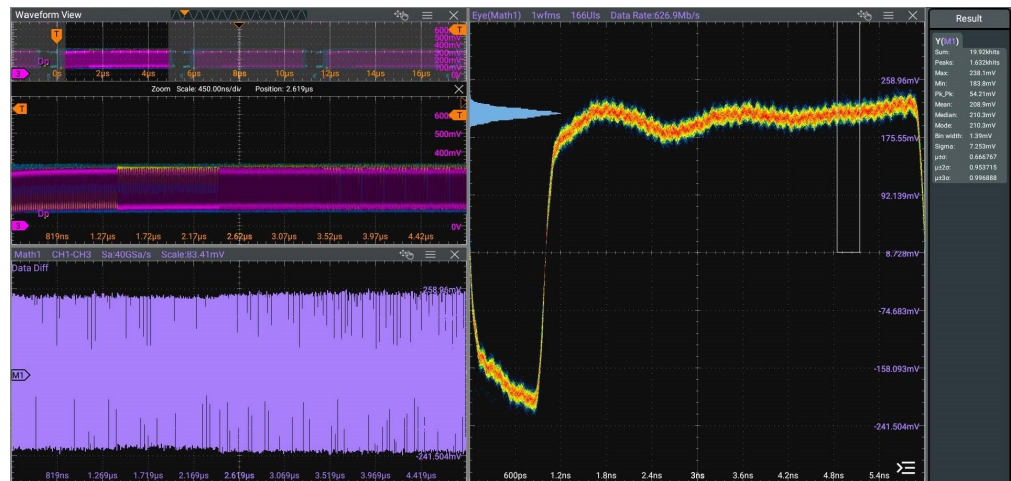


Figure 10.6 Test 1.3.4 Test Waveform and Result

Requirements

Figure 10.7 $V_{OD(1)}$ Test Result

10.6 Test 1.3.5 Data Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})

This test verifies whether the differential voltage mismatch (ΔV_{OD}) value of the DUT's data lane HS transmitter is within the conformance limit.

$$\Delta V_{OD} = |V_{OD(1)} - V_{OD(0)}|$$

This test item can be measured with the measurement result obtained from [Test 1.3.4](#).

Test Procedures

Configure the DUT to send a HS burst sequence, as shown in [Figure 10.1](#).

Refer to [Group3 Test Procedures](#) to perform the test.

If the DUT has the load impedance, connect the data lane to the $Z_{ID} = 125 \Omega$ and $Z_{ID} = 80 \Omega$ lane of the RTB, then repeat the above test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$ \Delta V_{OD} $			14 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

10.7 Test 1.3.6 Data Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$, $V_{OHHS(DN)}$)

This test verifies that the single-ended output high voltages ($V_{OHHS(DP)}$ and $V_{OHHS(DN)}$) of the DUT's data lane HS transmitter are within the conformance limit.

In this test, $V_{OHHS(DP)}$ is defined as the highest level of V_{Dp} at the Dn pin of data lane, and $V_{OHHS(DN)}$ is defined as the highest level of V_{Dn} at the Dn pin of data lane. Refer to measurement methods for [Test 1.3.4](#) to measure the single-ended signal level V_{Dp} and V_{Dn} .

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

If the DUT has the load impedance, connect the data lane to the $Z_{ID} = 125 \Omega$ and $Z_{ID} = 80 \Omega$ lane of the RTB, then repeat the above test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$V_{OHHS(Dp)}$			360 mV
$V_{OHHS(Dn)}$			360 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

Test Result Reference

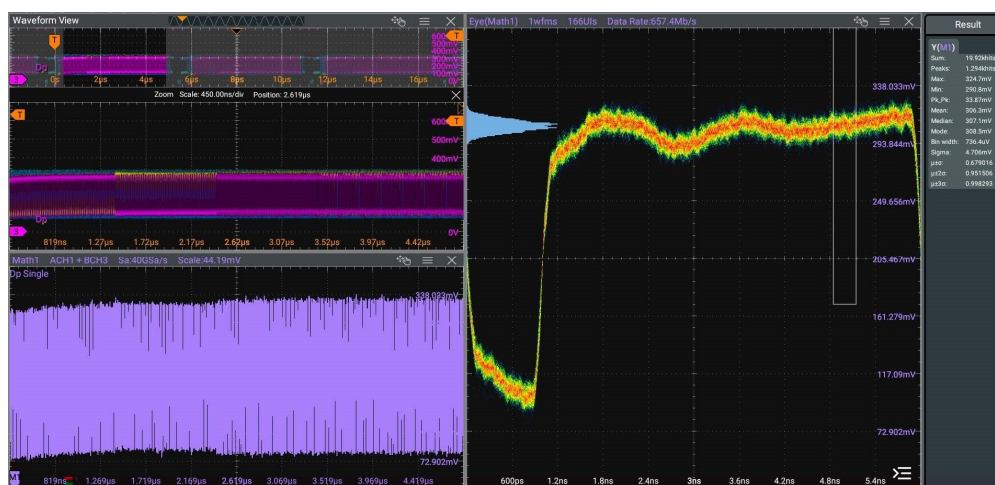
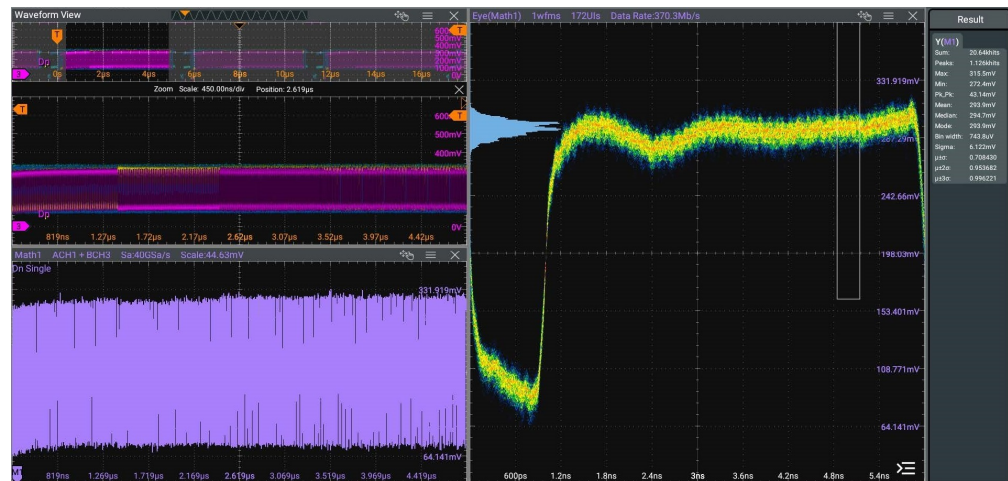


Figure 10.8 $V_{OHHS(Dp)}$ Test Result

Figure 10.9 $V_{OHHS(Dn)}$ Test Result

10.8 Test 1.3.7 Data Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}$, $V_{CMTX(0)}$)

This test verifies whether the static common-mode voltages ($V_{CMTX(1)}$ and $V_{CMTX(0)}$) of the DUT data lane HS transmitter are within the conformance limit.

The common-mode voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the Dp and Dn pins, as shown in the figure below.

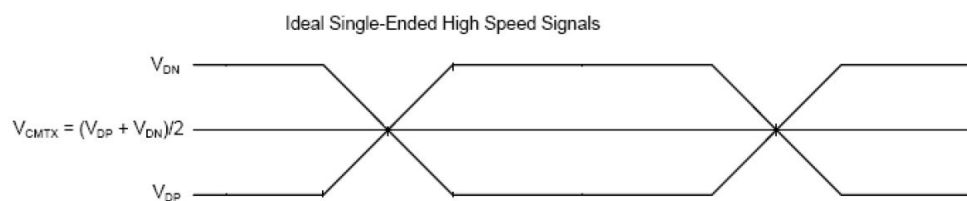


Figure 10.10 Ideal Single-ended and High Speed Signal

$$V_{CMTX} = (V_{DP} + V_{DN})/2$$

- $V_{CMTX(0)}$: indicates a device's HS-TX differential voltage level for the HS-0 state ($V_{Dp} < V_{Dn}$).
- $V_{CMTX(1)}$: indicates a device's HS-TX differential voltage level for the HS-1 state ($V_{Dp} > V_{Dn}$).

Test Procedures

Refer to *Group3 Test Procedures* to perform the test.

If the DUT has the load impedance, connect the data lane to the $Z_{ID} = 125 \Omega$ and $Z_{ID} = 80 \Omega$ lane of the RTB, then repeat the above test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$V_{\text{CMTX}(1)}$		150 mV	250 mV
$V_{\text{CMTX}(0)}$		150 mV	250 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

Test Result Reference

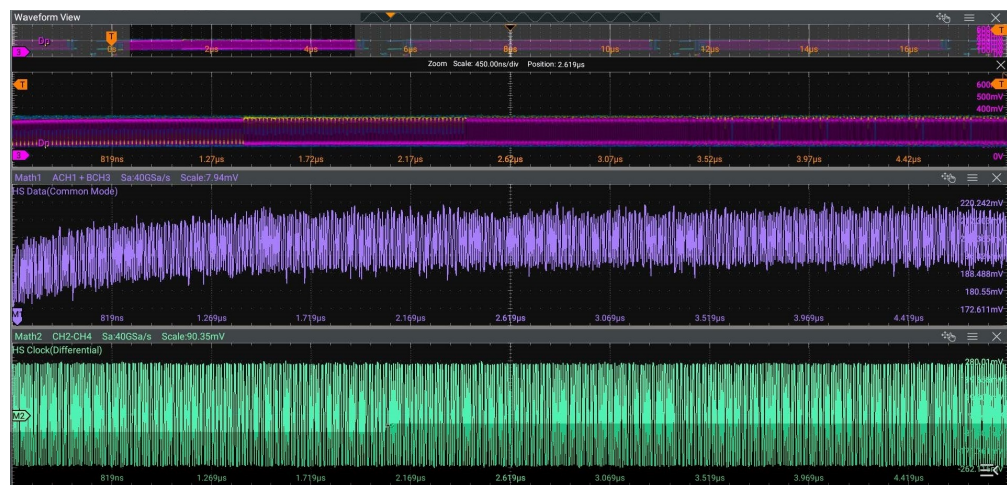


Figure 10.11 ($V_{\text{CMTX}(1)}$, $V_{\text{CMTX}(0)}$) Test Result

10.9 Test 1.3.8 Data Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{\text{CMTX}(1,0)}$)

This test verifies whether the static common-mode voltage mismatch ($\Delta V_{\text{CMTX}(1,0)}$) of the DUT data lane HS transmitter is within the conformance limit.

Use the value $V_{\text{CMTX}(1)}$ and $V_{\text{CMTX}(0)}$ obtained from [Test 1.3.7](#) Data Lane HS-TX Static Common-Mode Voltages. The result for $\Delta V_{\text{CMTX}(1,0)}$ is computed as one-half of the difference of $V_{\text{CMTX}(1)}$ minus $V_{\text{CMTX}(0)}$.

$$\Delta V_{\text{CMTX}(1,0)} = (V_{\text{CMTX}(1)} - V_{\text{CMTX}(0)})/2$$

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

If the DUT has the load impedance, connect the data lane to the $Z_{\text{ID}} = 125 \Omega$ and $Z_{\text{ID}} = 80 \Omega$ lane of the RTB, then repeat the above test.

Requirements

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$ \Delta V_{\text{CMTX}(1,0)} $			5 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

10.10 Test 1.3.9 Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ($\Delta V_{\text{CMTX(LF)}}$)

This test verifies that the AC Common-Mode Signal Level Variations between 50 MHz and 450 MHz ($\Delta V_{\text{CMTX(LF)}}$) of the DUT data lane HS transmitter are less than the maximum allowable limit.

Due to the signal distortion, there is rise time/fall time asymmetry for the single-ended HS signals on the data lane. The AC common-mode signal level will change, and the low frequency common-mode voltage variation is expressed as $\Delta V_{\text{CMTX(LF)}}$. Refer to measurement methods for [Test 1.3.7](#) to measure the common-level variations between 50 MHz and 450 MHz and obtain the value of $V_{\text{CMTX(LF)}}$.

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$\Delta V_{\text{CMTX(LF)}}$			25 mV _{PEAK}

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 20 and Figure 43.

Test Result Reference



Figure 10.12 Test 1.3.9 Test Waveform and Result

10.11 Test 1.3.10 Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{\text{CMTX(HF)}}$)

This test verifies that the AC Common-Mode Signal Level Variations above 450 MHz ($\Delta V_{\text{CMTX(HF)}}$) of the DUT data lane HS transmitter are less than the maximum allowable limit.

Due to the signal distortion, there is rise time/fall time asymmetry for the single-ended HS signals on the data lane. The AC common-mode signal level will change, and the dynamic common-mode voltage level is expressed as $\Delta V_{\text{CMTX(HF)}}$. Refer to measurement methods for [Test 1.3.7](#) to measure the common-level variations above 450MHz $V_{\text{CMTX(HF)}}$.

Test Procedures

Configure the DUT to send a HS burst sequence, as shown in [Figure 10.1](#). Refer to [Group3 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$\Delta V_{\text{CMTX(HF)}}$			15 mV _{RMS}

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 20.

Test Result Reference

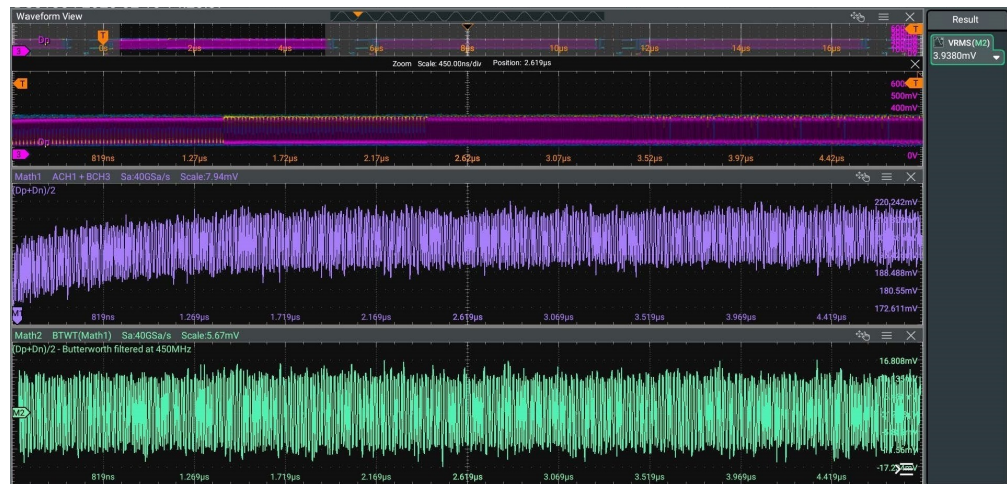


Figure 10.13 Test 1.3.10 Test Waveform and Result

10.12 Test 1.3.11 Data Lane HS-TX 20%-80% Rise Time (t_R)

This test verifies whether the 20%-80% Rise Time (t_R) value of the DUT's clock lane LP transmitter is within the conformance limit.

Refer to measurement methods for [Test 1.3.4](#) to measure $V_{OD(0)}$ and $V_{OD(1)}$. Then measure the 20%-80% Rise Time (t_R) based on the values.

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

If the DUT has the load impedance, connect the data lane to the $Z_{ID} = 125 \Omega$ and $Z_{ID} = 80 \Omega$ lane of the RTB, then repeat the above test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
t_R	≤ 1 Gbps		$0.30 \cdot UI$
	> 1 Gbps and ≤ 1.5 Gbps		$0.35 \cdot UI$
	> 1.5 Gbps		$0.4 \cdot UI$

Wherein, UI is the nominal HS Unit Interval for the DUT, see [Test 1.4.17](#).

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 20.

Test Result Reference

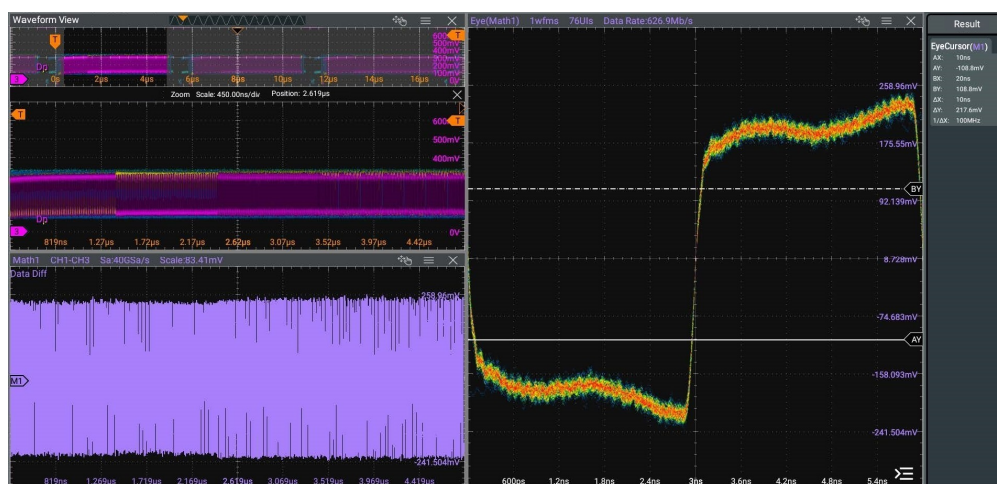


Figure 10.14 Test 1.3.11 Test Waveform and Result

10.13 Test 1.3.12 Data Lane HS-TX 80%-20% Fall Time (t_F)

This test verifies whether the 80%-20% Fall Time (t_F) value of the DUT's clock lane LP transmitter is within the conformance limit.

Refer to measurement methods for [Test 1.3.4](#) to measure $V_{OD(0)}$ and $V_{OD(1)}$. Then measure the 80%-20% Fall Time (t_F) based on the values.

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

If the DUT has the load impedance, connect the data lane to the $Z_{ID} = 125 \Omega$ and $Z_{ID} = 80 \Omega$ lane of the RTB, then repeat the above test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
t_F	≤ 1 Gbps		$0.30 \cdot UI$
	> 1 Gbps and ≤ 1.5 Gbps		$0.35 \cdot UI$
	> 1.5 Gbps		$0.4 \cdot UI$

Wherein, UI is the nominal HS Unit Interval for the DUT, see [Test 1.4.17](#).

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 20.

Test Result Reference



Figure 10.16 Test 1.3.13 Test Waveform and Result

10.15 Test 1.3.14 Data Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})

This test verifies whether the 30%-85% Post-EoT Rise Time (T_{REOT}) value of the DUT's clock lane LP transmitter is within the conformance limit.

As shown in [Figure 10.1](#), to exit the HS burst state, the data lane needs to send the EoT sequence and then go back to Stop state (LP-11). Refer to measurement methods for [Test 1.3.4](#) to measure V_{OD} , measure a device's LP-TX 30%--85% Rise Time to obtain T_{REOT} .

Test Procedures

Refer to [Group3 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
T_{REOT}			35 ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.12, Table 22.

Test Result Reference



Figure 10.17 Test 1.3.14 Test Waveform and Result

10.16 Test 1.3.15 Data Lane HS Exit: T_{EOT} Value

This test verifies that the combined duration of the THS-TRAIL plus T_{REOT} intervals of the DUT data lane transmitter is less than the maximum allowable value.

As shown in *Figure 10.1*, $T_{EOT} = T_{HS-TRAIL} + T_{REOT}$. Use the values $T_{HS-TRAIL}$ and T_{REOT} obtained from *Test 1.3.13* and *Test 1.3.14*.

Test Procedures

Refer to *Group3 Test Procedures* to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
T _{EOT}			105 ns + 12*UI

Wherein, UI is the nominal HS Unit Interval for the DUT, see *Test 1.4.17*.

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.7, Table 14.

Test Result Reference



Figure 10.18 Test 1.3.15 Test Waveform and Result

10.17 Test 1.3.16 Data Lane HS Exit: $T_{HS-EXIT}$ Value

This test verifies that the duration that the data lane transmitter remains in the Stop (LP-11) state after exiting HS mode (THS-EXIT), is greater than the minimum required value.

To exit the HS burst state, the data lane needs to send the EoT sequence and then go back to Stop state (LP-11). The D-PHY Specification provides a requirement for the minimum time that the lane must remain in the Stop (LP-11) state before initiating any further sequences. The interval is defined as $T_{HS-EXIT}$, as shown in *Figure 10.1*.

Test Procedures

Refer to *Group3 Test Procedures* to perform the test.

Pass Conditions

The test results shall meet the following conditions: $T_{HS-EXIT} \geq 100$ ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.7, Table 14.

Requirements

Test Result Reference



Figure 10.19 Test 1.3.16 Test Waveform and Result

11 Group 4 Clock Lane HS-TX Signaling Requirements

This section introduces the test methods for the test items of Group4 when you select "Normal" or "Normal+Escape" as the test mode in *System Settings*. If you select "Continuous Data" as the clock mode, refer to descriptions in *Continuous Data Test Mode*.

This group of tests verifies various requirements specific to Clock Lane HS-TX signaling.

For this group of tests, configure the data lane of the DUT to enter the high-speed burst data transmission state, as shown in the figure below.

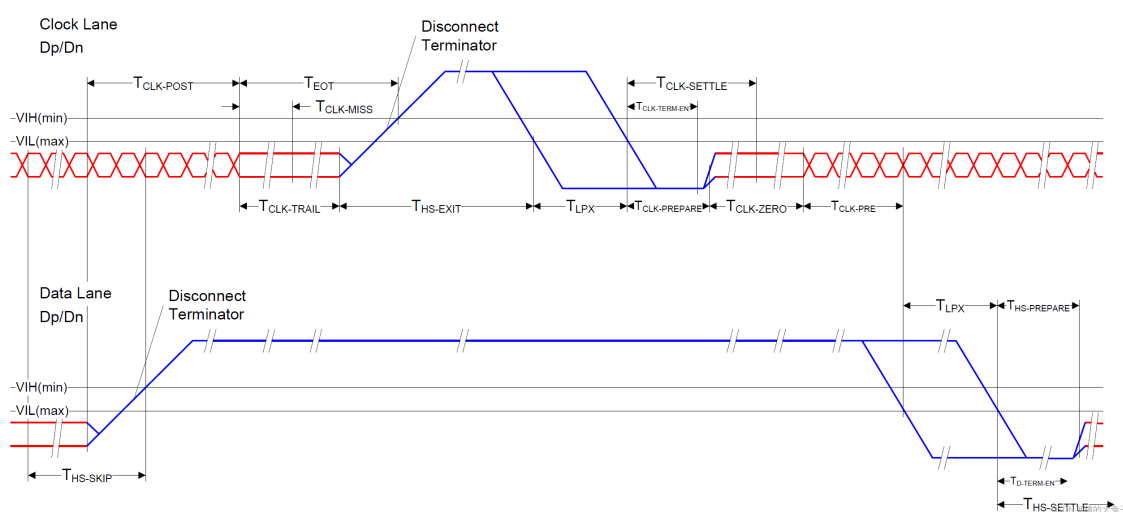


Figure 11.1 Switch the Clock Lane between Clock Transmission and Low-Power Mode

- Sequence when the clock lane enters the high-speed mode (HS Entry): LP11->LP10(T_{LPX})->LP00($T_{CLK-PREPARE}$)->HS0($T_{CLK-ZERO}$)-> $T_{CLK-PRE}$
- Sequence when the clock lane exits the high-speed mode (HS Exit): HS0/HS1-> $T_{CLK-POST}$ end with HS0-> $T_{CLK-TRAIL}$ ->LP-11($T_{HS-EXIT}$)

NOTE

This group of tests are generally performed on the master DUT, and they are not available for slave DUT.

11.1 Group4 Test Procedures

Configure the oscilloscope to perform the MIPI compliance test.

Open the MIPI compliance test interface, as shown in *Figure 6.1*.

1. Click or tap the "System Settings" tab to configure the test.
 - Select the desired D-PHY version and High-Speed Rate according to the actual situation of the DUT.
 - Select "Escape" or "Normal+Escape" from the drop-down button of "Test Mode".
 - Click or tap the drop-down button of **Clock Mode** to select "Normal".
 - Based on the test device connection, select "CH1" as the D+ source and "CH3" as the D- source of the Data Lane. Select "CH2" as the D+ source and "CH4" as the D- source of the Clock Lane.

For the different configurations in the "System Settings" tab for the test items of Group4, refer to descriptions in *Table 6.5 Different Scenarios for Different Test Items of Group4*.

2. Click or tap the "Test Item" tab, and check the checkbox of Group4 and all of test items under it.
3. Observe the specified waveform sequence captured by the oscilloscope on the clock lane.
4. Click or tap the "Analysis Settings" tab. Click or tap **Start** to perform the test according to its instructions.
5. Click or tap the "Result Export" tab to configure the result export, save and export the report.

Analyze the test report, and observe the test results for each test item.

11.2 Test 1.4.1 Clock Lane HS Entry: Clock Lane T_{LPX} Value

This test verifies that the duration T_{LPX} of the final clock lane LP-01 state immediately before HS transmission is greater than the minimum conformance value.

The test method for this test is similar with that for *Test 1.3.1 Data Lane T_{LPX} Value* except that it is performed on the clock lane T_{LPX} interval, as shown in *Figure 11.1*.

Test Procedures

Refer to *Group4 Test Procedures* to perform the test.

Pass Conditions

The test results shall meet the following conditions: $T_{LPX} \geq 50$ ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.2, Table 14.

Test Result Reference

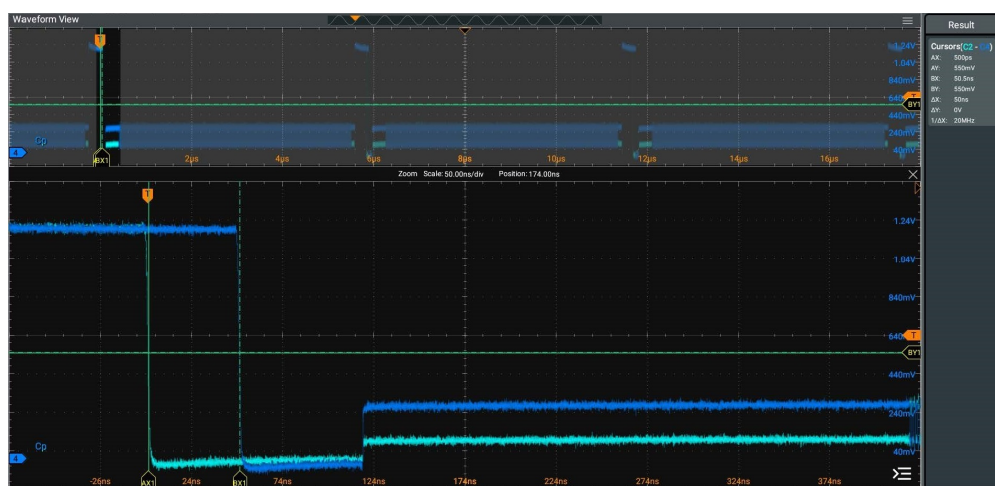


Figure 11.2 Test 1.4.1 Test Waveform and Result

11.3 Test 1.4.2 Clock Lane HS Entry: $T_{CLK-PREPARE}$ Value

This test verifies that the time that the DUT clock lane transmitter drives LP-00 ($T_{CLK-PREPARE}$) prior to driving $T_{CLK-ZERO}$ when entering the HS mode, is within the conformance limit.

The test method for this test is similar with that for *Test 1.3.2 Data Lane $T_{HS-PREPARE}$ Value* except that it is performed on the clock lane $T_{HS-PREPARE}$ interval, as shown in *Figure 11.1*.

Test Procedures

Configure the DUT to send high-speed burst signal on the clock lane, as shown in *Figure 11.1*.

Refer to *Group4 Test Procedures* to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Requirements

Parameter	DUT Rate	Min.	Max.
$T_{\text{HS-PREPARE}}$		38 ns	95 ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.9, Table 14.

Test Result Reference

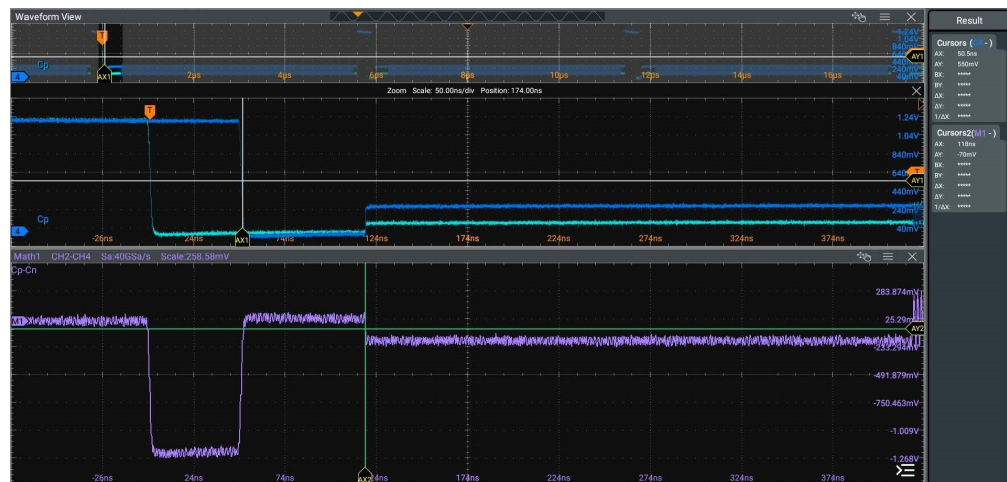


Figure 11.3 Test 1.4.2 Test Waveform and Result

11.4 Test 1.4.3 Clock Lane HS Entry: $T_{\text{CLK-PREPARE}} + T_{\text{CLK-ZERO}}$ Value

This test verifies that the combined time of $T_{\text{CLK-PREPARE}}$ plus $T_{\text{CLK-ZERO}}$ is greater than the minimum required value.

- For the definition and test method of $T_{\text{CLK-PREPARE}}$, refer to [Test 1.4.2](#).
- $T_{\text{CLK-ZERO}}$ is defined as the minimum duration that the DUT clock lane transmitter drives the extended HS-0 differential state (TCLK-ZERO) prior to starting clock transmission.

The test method for this test is similar with that for [Test 1.3.3](#) Data Lane $T_{\text{CLK-ZERO}}$ Value except that it is performed on the clock lane, as shown in [Figure 11.1](#).

Pass Conditions

Configure the DUT to send high-speed burst signal on the clock lane, as shown in [Figure 11.1](#).

The test results shall meet the following conditions: $(T_{\text{CLK-PREPARE}} + T_{\text{CLK-ZERO}}) \geq 300 \text{ ns}$

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.9, Table 14.

Test Result Reference



Figure 11.4 Test 1.4.3 Test Waveform and Result

11.5 Test 1.4.4 Clock Lane HS-TX Differential Voltages ($V_{OD(0)}$, $V_{OD(1)}$)

This test verifies whether the differential voltages ($V_{OD(0)}$ and $V_{OD(1)}$) of the DUT's clock lane HS transmitter are within the conformance limit.

The differential output voltage V_{OD} is defined as the difference of voltages V_{Dp} and V_{Dn} at the Dp and Dn pins, respectively. The test method for this test is similar with that for [Test 1.3.4](#), except that it is performed on the clock lane, as shown in [Figure 11.1](#).

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Pass Conditions

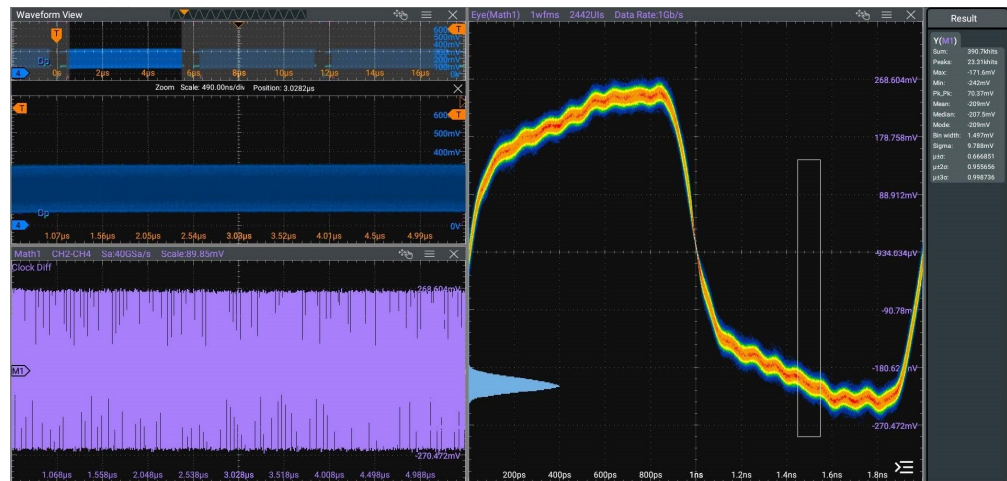
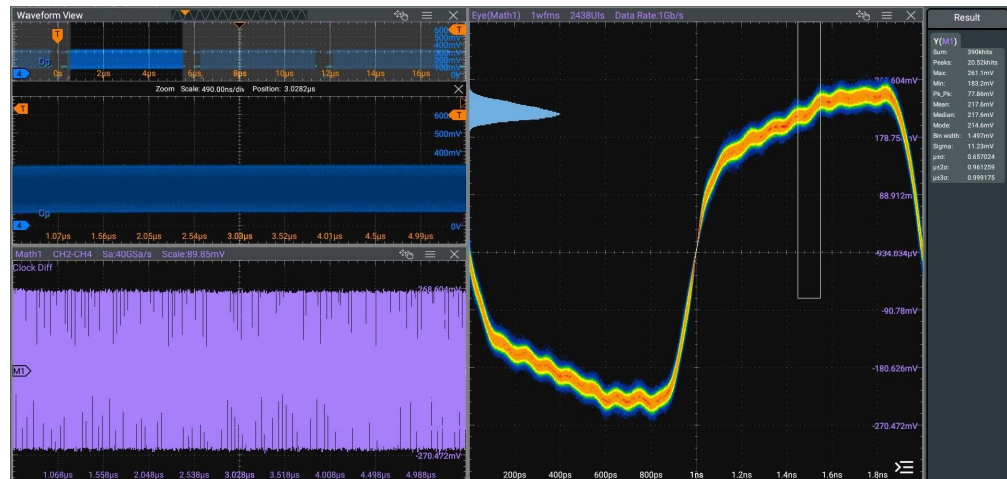
The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$V_{OD(1)}$		140 mV	270 mV
$V_{OD(0)}$		-270 mV	-140 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

Test Result Reference

Figure 11.5 $V_{OD(0)}$ Test Waveform and ResultFigure 11.6 $V_{OD(1)}$ Test Waveform and Result

11.6 Test 1.4.5 Clock Lane HS-TX Differential Voltage Mismatch (ΔV_{OD})

This test verifies whether the differential voltage mismatch (ΔV_{OD}) of the DUT's clock lane HS transmitter is within the conformance limit.

The differential output voltage V_{OD} is defined as the difference of voltages V_{Dp} and V_{Dn} at the Dp and Dn pins, respectively. The test method for this test is similar with that for [Test 1.3.5](#), except that it is performed on the clock lane, as shown in [Figure 11.1](#).

Test Procedures

Refer to *Group4 Test Procedures* to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$ \Delta V_{OD} $			14 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

11.7 Test 1.4.6 Clock Lane HS-TX Single-Ended Output High Voltages ($V_{OHHS(DP)}$, $V_{OHHS(DN)}$)

This test verifies that the single-ended output high voltages ($V_{OHHS(DP)}$ and $V_{OHHS(DN)}$) of the DUT's clock lane HS transmitter are within the conformance limit.

V_{OHHS} is defined as a device's HS-TX output high voltage. The test method for this test is similar with that for *Test 1.3.6*, except that it is performed on the clock lane, as shown in *Figure 11.1*.

Test Procedures

Refer to *Group4 Test Procedures* to perform the test.

Pass Conditions

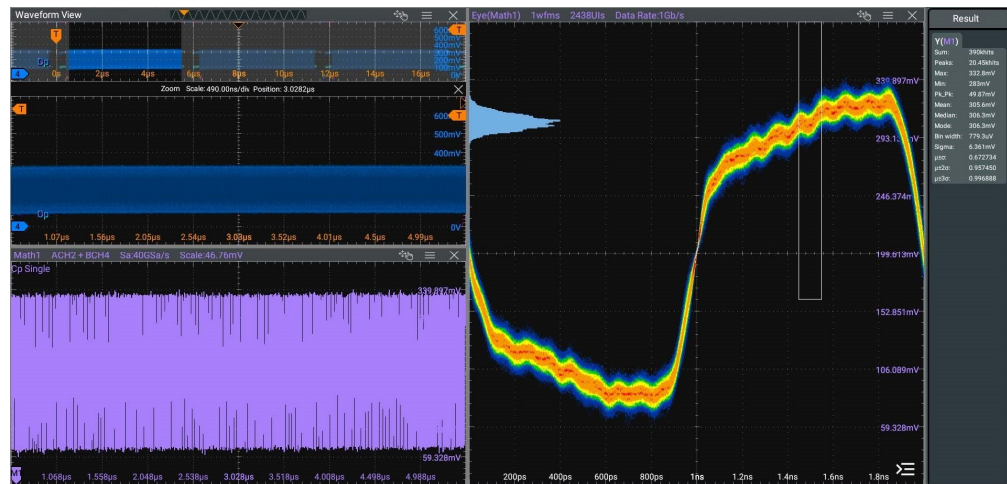
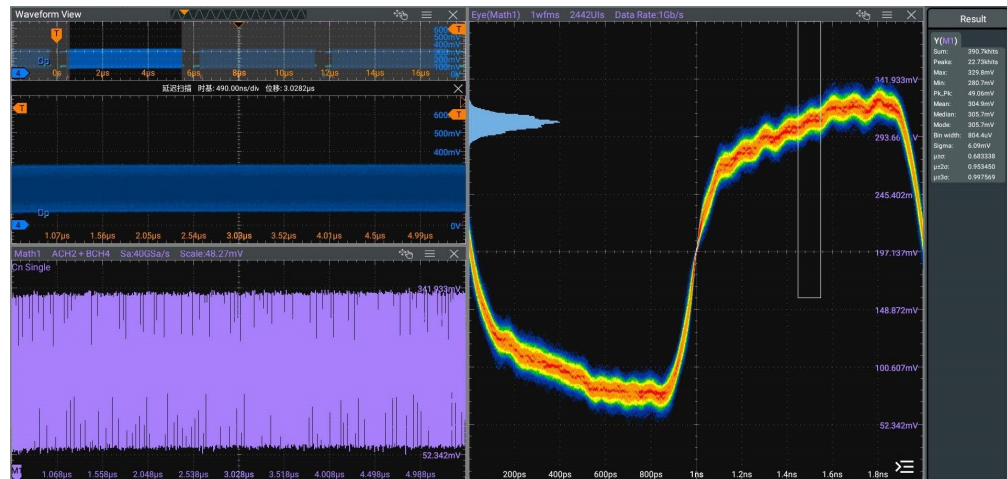
This test shall meet the following conditions, with all the three Z_{ID} cases.

Parameter	DUT Rate	Min.	Max.
$V_{OHHS(Dp)}$			360 mV
$V_{OHHS(Dn)}$			360 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

Test Result Reference

Figure 11.7 $V_{OHHS(DP)}$ Test Waveform and ResultFigure 11.8 $V_{OHHS(DN)}$ Test Waveform and Result

11.8 Test 1.4.7 Clock Lane HS-TX Static Common-Mode Voltages ($V_{CMTX(1)}$, $V_{CMTX(0)}$)

This test verifies whether the static common-mode voltages ($V_{CMTX(1)}$ and $V_{CMTX(0)}$) of the DUT clock lane HS transmitter are within the conformance limit.

The common-mode voltage V_{CMTX} is defined as the arithmetic mean value of the voltages at the Clkp and Clkn pins. The test method for this test is similar with that for [Test 1.3.7](#), except that it is performed on the clock lane.

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$V_{\text{CMTX}(1)}$		150 mV	250 mV
$V_{\text{CMTX}(0)}$		150 mV	250 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

Test Result Reference

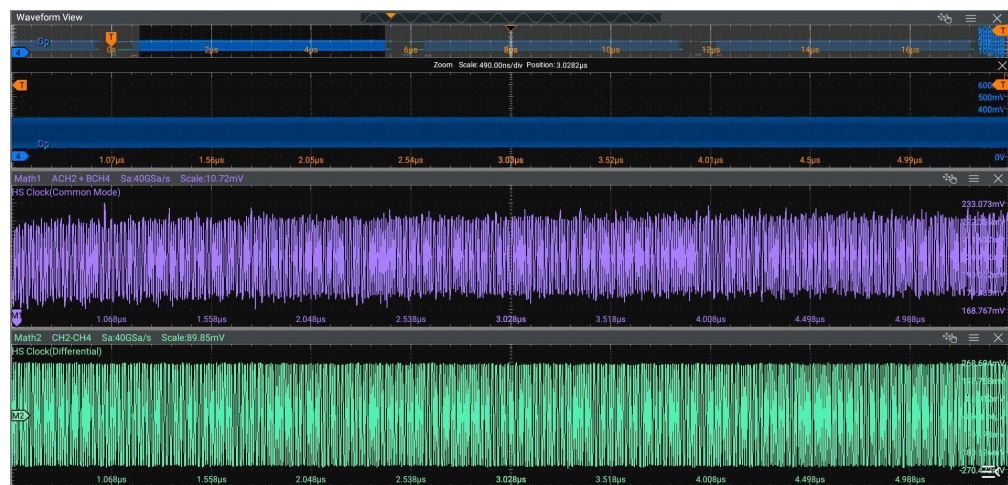


Figure 11.9 Test 1.4.7 Test Waveform and Result

11.9 Test 1.4.8 Clock Lane HS-TX Static Common-Mode Voltage Mismatch ($\Delta V_{\text{CMTX}(1,0)}$)

This test verifies whether the static common-mode voltage mismatch ($\Delta V_{\text{CMTX}(1,0)}$) of the DUT's clock lane HS transmitter is within the conformance limit.

The test method for this test is similar with that for [Test 1.3.8](#) Data Lane $\Delta V_{\text{CMTX}(1,0)}$, except that it is performed on the clock lane $V_{\text{CMTX}(1,0)}$.

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Requirements

Parameter	DUT Rate	Min.	Max.
$ \Delta V_{\text{CMTX}(1,0)} $			5 mV

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 19.

11.10 Test 1.4.9 Clock Lane HS-TX Dynamic Common-Level Variations Between 50 MHz-450MHz ($\Delta V_{\text{CMTX}(\text{LF})}$)

This test verifies that the AC Common-Mode Signal Level Variations between 50 MHz and 450 MHz ($\Delta V_{\text{CMTX}(\text{LF})}$) of the DUT clock lane HS transmitter are less than the maximum allowable limit.

$V_{\text{CMTX}(\text{LF})}$ is defined as a device's HS-TX Dynamic Common-Level Variations between 50 MHz and 450 MHz. The test method for this test is similar with that for [Test 1.3.9](#), except that it is performed on the clock lane, as shown in [Figure 11.1](#).

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$\Delta V_{\text{CMTX}(\text{LF})}$			25 mV _{PEAK}

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 20.

Test Result Reference



Figure 11.10 Test 1.4.9 Test Waveform and Result

11.11 Test 1.4.10 Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz ($\Delta V_{\text{CMTX(HF)}}$)

This test verifies that the AC Common-Mode Signal Level Variations above 450 MHz ($\Delta V_{\text{CMTX(LF)}}$) of the DUT clock lane HS transmitter are less than the maximum allowable limit.

The test method for this test is similar with that for [Test 1.3.10](#) Data Lane $\Delta V_{\text{CMTX(HF)}}$, except that it is performed on the clock lane. The conformance limits are the same as the data lane case.

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$\Delta V_{\text{CMTX(HF)}}$			15 mV _{RMS}

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 20.

Test Result Reference

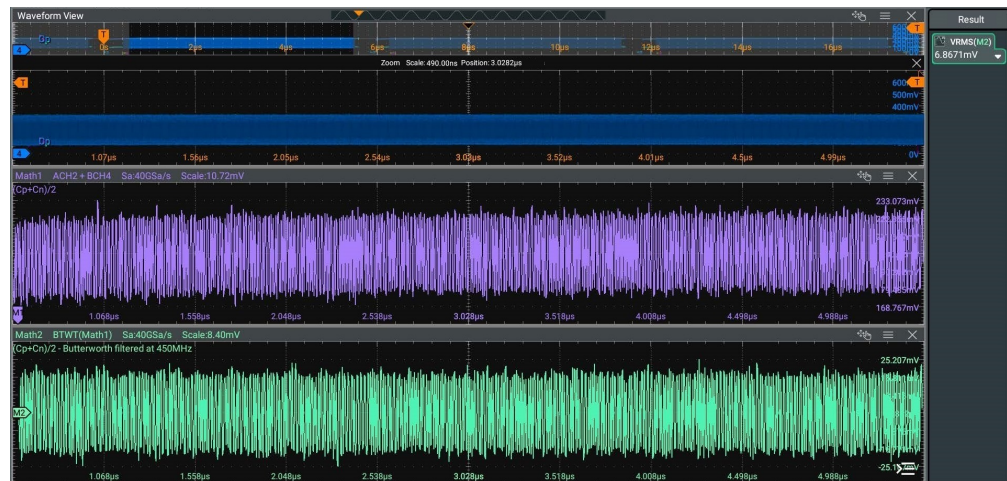


Figure 11.11 Test 1.4.10 Test Waveform and Result

11.12 Test 1.4.11 Clock Lane HS-TX 20%-80% Rise Time (t_R)

This test verifies whether the 20%-80% Rise Time (t_R) value of the DUT's clock lane HS transmitter is within the conformance limit.

The test method in this test is similar with that for the [Test 1.3.11](#). A similar methodology is used to create an averaged waveform on which the measurement is performed. However, rather than using a 000111 reference data pattern, a 01 pattern is used (as 000111 pattern does not exist on the clock lane). The reference top and base levels shall be determined from the clock lane settled DC HS-ZERO level, i.e., $V_{HS-ZERO}$.

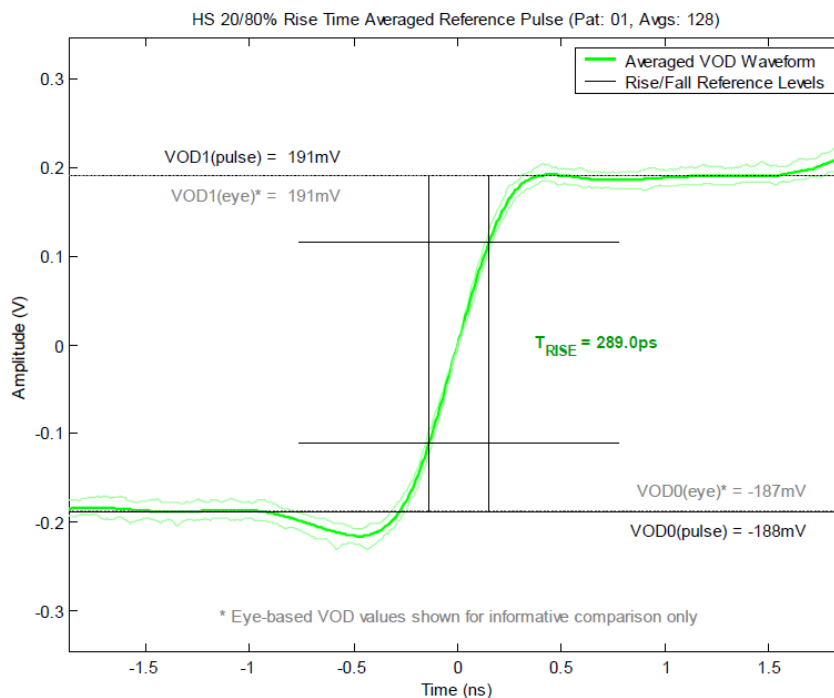


Figure 11.12 Sample Clock Lane HS Rise Time Reference Waveform and Measurement

Test Procedures

Refer to *Group4 Test Procedures* to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
t_R	≤ 1 Gbps		$0.30 \cdot UI$
	> 1 Gbps and ≤ 1.5 Gbps		$0.35 \cdot UI$
	> 1.5 Gbps		$0.4 \cdot UI$

Wherein, UI is the nominal HS Unit Interval for the DUT, see *Test 1.4.17*.

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 20.

Test Result Reference

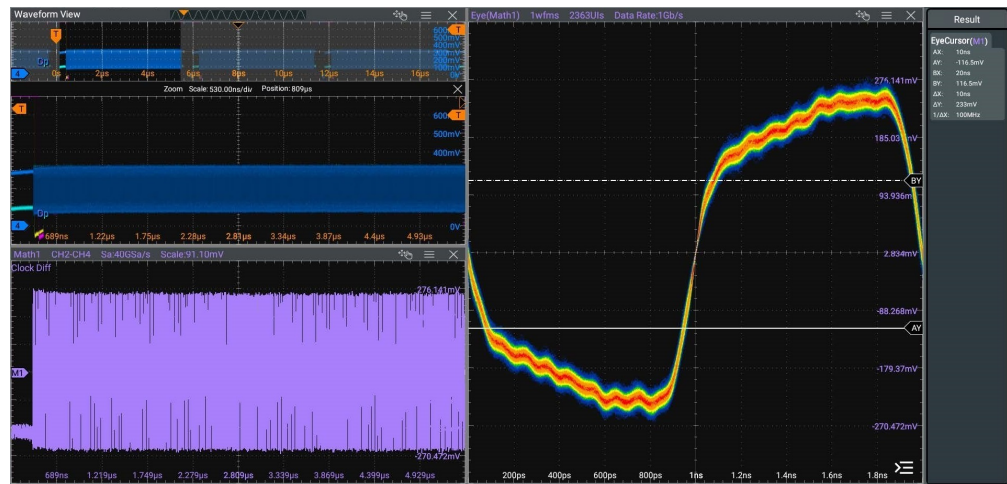


Figure 11.13 Test 1.4.11 Test Waveform and Result

11.13 Test 1.4.12 Clock Lane HS-TX 80%-20% Fall Time (t_F)

This test verifies whether the 80%-20% Rise Time (t_F) value of the DUT's clock lane HS transmitter is within the conformance limit.

The test method for this test is similar with that for [Test 1.4.11](#) for rise time, except the fall time measured on a reference 10 data pattern. The reference top and base levels are still the clock lane $V_{HS-ZERO}$ values measured in the previous test.

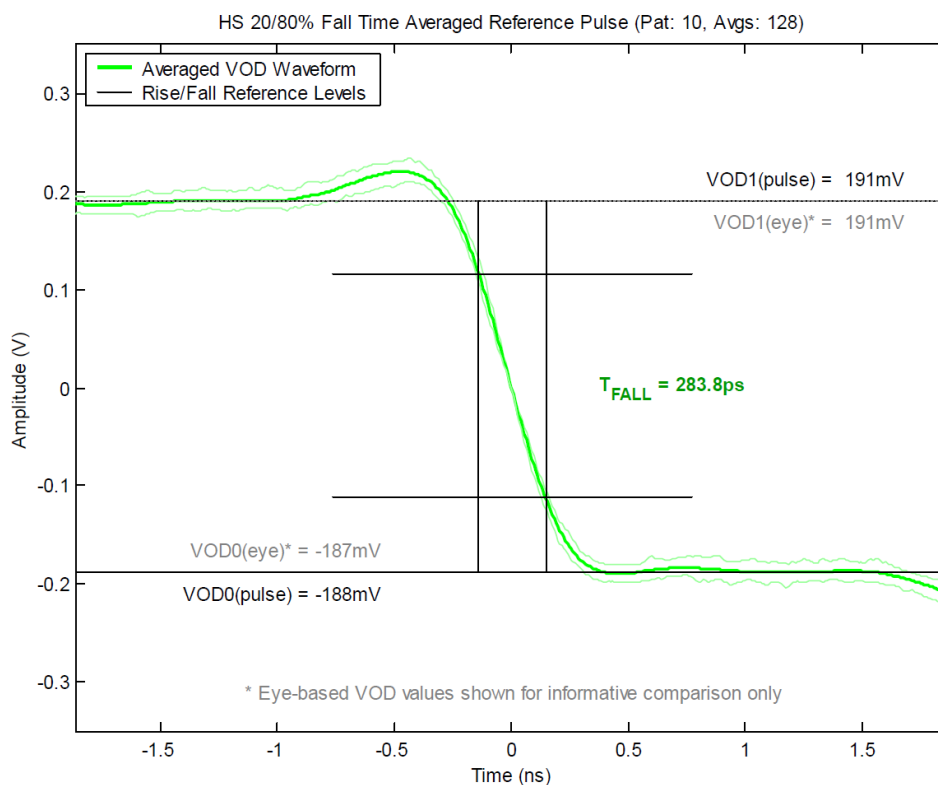


Figure 11.14 Sample Clock Lane HS Fall Time Reference Waveform and Measurement

Test Procedures

Refer to *Group4 Test Procedures* to perform the test.

Pass Conditions

This measurement will be performed for the $Z_{ID} = 80\ \Omega$ and $100\ \Omega$ cases. In v1.0, all the cases are required to be tested. But for the versions above 1.0, $125\ \Omega$ is not a required case, only $80\ \Omega$ and $100\ \Omega$ case tests are required to be performed.

	DUT Rate	Min.	Max.
t_F	$\leq 1\ \text{Gbps}$		$0.30 \cdot UI$
	$> 1\ \text{Gbps}$ and $\leq 1.5\ \text{Gbps}$		$0.35 \cdot UI$
	$> 1.5\ \text{Gbps}$		$0.4 \cdot UI$

Wherein, UI is the nominal HS Unit Interval for the DUT, see *Test 1.4.17*.

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 9.1.1, Table 20.

Test Result Reference

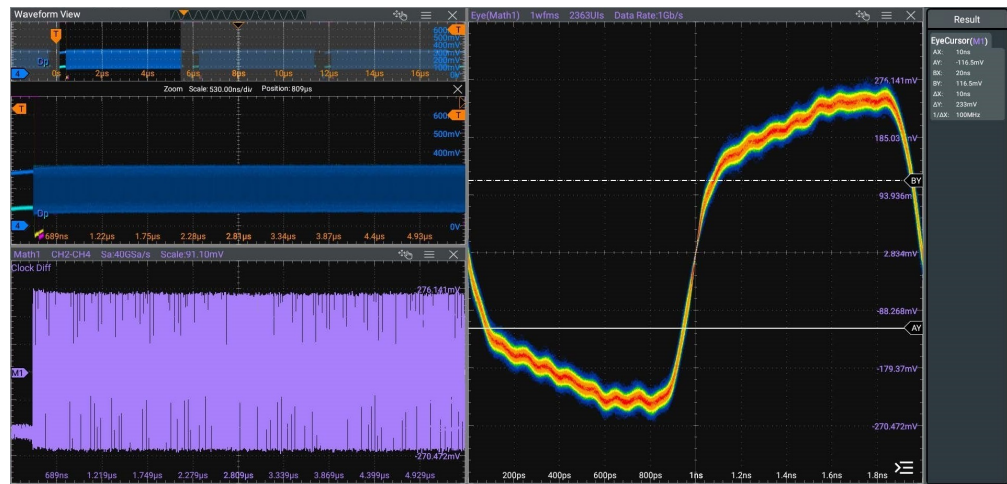


Figure 11.15 Test 1.4.11 Test Waveform and Result

11.14 Test 1.4.13 Clock Lane HS Exit: T_{CLK-TRAIL} Value

This test verifies that the duration of the DUT clock lane HS transmitter drives the inverted final differential state following the last payload data bit of a HS-TX burst ($T_{CLK-TRAIL}$) is greater than the minimum required value.

As part of the process for switching the clock lane out of HS mode, the D-PHY Specification provides a requirement for the duration of the final extended clock lane HS-0 state following the last payload clock bit of a HS transmission burst. This interval is defined as $T_{CLK-TRAIL}$, as shown in [Figure 11.1](#). The test method for this test is similar with that for [Test 1.3.13](#) for data lane $T_{HS-TRAIL}$, except that it is performed on the clock lane.

Test Procedures

Refer to *Group4 Test Procedures* to perform the test.

Pass Conditions

For $Z_{ID} = 100 \, \Omega$:

Parameter	DUT Rate	Min.	Max.
T _{CLK-TRAIL}		60 ns	

Reference Protocol

Refer to D-PHY Specification (v1.2), Table 10 and Table 14.

Test Result Reference



Figure 11.16 Test 1.4.13 Test Waveform and Result

11.15 Test 1.4.14 Clock Lane HS Exit: 30%-85% Post-EoT Rise Time (T_{REOT})

This test verifies that the 30%-85% Post-EoT Rise Time (T_{REOT}) value of the DUT's clock lane LP transmitter is within the conformance limit.

The test method for this test is similar with that for [Test 1.3.14](#) for data lane T_{REOT} , except that it is performed on the clock lane, as shown in [Figure 11.1](#).

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
T_{REOT}			35 ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.12, Table 22.

Test Result Reference



Figure 11.17 Test 1.4.14 Test Waveform and Result

11.16 Test 1.4.15 Clock Lane HS Exit: T_{EOT} Value

This test verifies the interval measured from the start of the DUT clock lane HS transmitter's $T_{CLK-TRAIL}$ to the start of the first Clock lane LP-11 state (T_{EOT}) is less than the maximum allowable value.

Configure the DUT to send the HS Exit sequence on the clock lane, as shown in [Figure 11.1](#). Use the values for $T_{CLK-TRAIL}$ and clock lane T_{REOT} obtained from [Test 1.4.13](#) and [Test 1.4.14](#). Add the two values together to obtain T_{EOT} . $T_{EOT} = T_{CLK-TRAIL} + T_{REOT}$.

The test method for this test is similar with that for [Test 1.3.15](#) for data lane T_{EOT} , except that it is performed on the clock lane. The conformance limits are the same as the data lane case.

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
T_{EOT}			105 ns + 12*UI

Wherein, UI is the nominal HS Unit Interval for the DUT, see [Test 1.4.17](#).

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.7, Table 14.

Test Result Reference



Figure 11.18 Test 1.4.15 Test Waveform and Result

11.17 Test 1.4.16 Clock Lane HS Exit: $T_{HS-EXIT}$ Value

This test verifies that the duration that the clock lane transmitter remains in the Stop (LP-11) state after exiting HS mode ($T_{HS-EXIT}$) is greater than the minimum required value.

The test method for this test is similar with that for [Test 1.3.16](#) for data lane $T_{HS-EXIT}$, except that it is performed on the clock lane.

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions: $T_{HS-EXIT} \geq 100$ ns

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.7, Table 14.

Test Result Reference

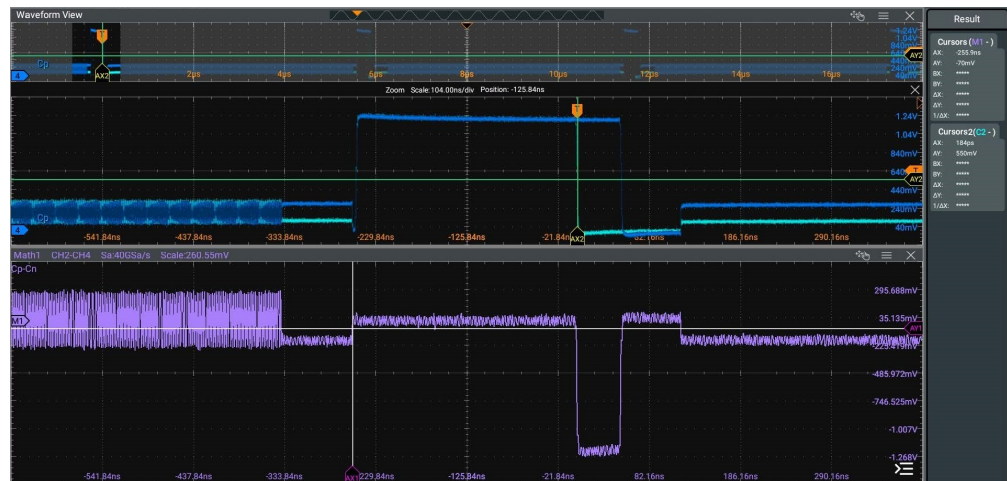
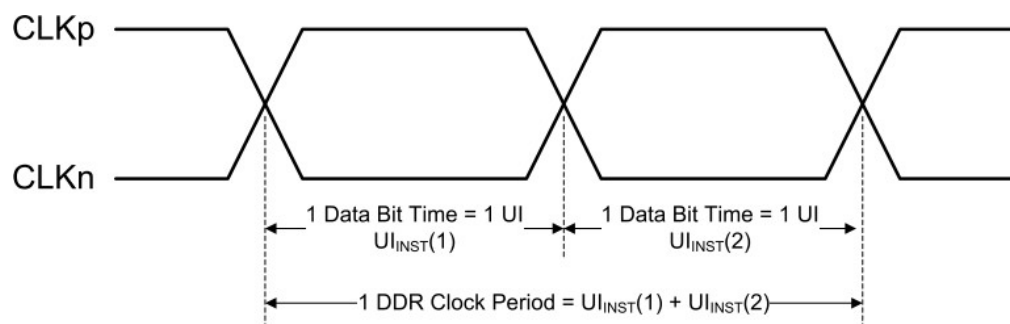


Figure 11.19 Test 1.4.16 Test Waveform and Result

11.18 Test 1.4.17 Clock Lane HS Clock Instantaneous UI (U_{INST})

This test verifies that the Instantaneous Unit Interval (U_{INST}) value of the DUT's clock lane HS transmitter is within the conformance limit.

This test requires to test the differential clock signal. For example, if the current waveform is the clock single-ended signal, then construct the differential clock waveform by using the equation: $V_{CLKP} - V_{CLKN}$. Measure the HS clock signal sent from the DUT clock lane. The following figure shows one DDR clock period. The U_{INST} values for each UI will be measured as the difference between two successive 0 V crossing times of the differential waveform. The sample shall contain a minimum of 5,000 UIs.

Figure 11.20 U_{INST} Interval

Test Procedures

Refer to [Group4 Test Procedures](#) to perform the test.

Before performing test, obtain the $UI_{INST,MIN}$ value from the DUT vendor to modify the parameter range in *Specification Management* specified for Test 1.4.17.

Pass Conditions

The test results shall meet the following conditions:

- $UI_{INST} < 12.5 \text{ ns}$
- $UI_{INST} \geq UI_{INST,MIN}$ value from the DUT vendor

You can obtain the $UI_{INST,MIN}$ value from the DUT vendor or DUT Datasheet.

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 10.1, Table 29.

Test Result Reference

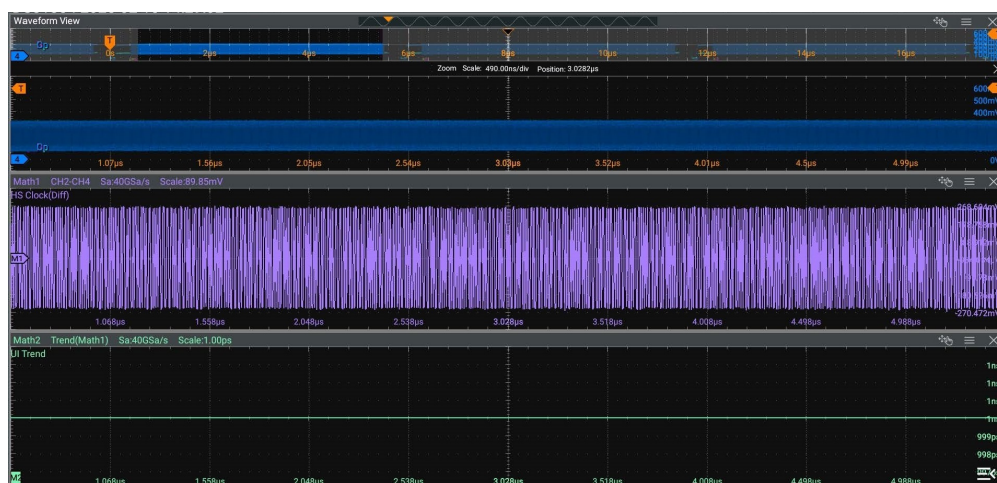


Figure 11.21 Test 1.4.17 Test Waveform and Result

11.19 Test 1.4.18 Clock Lane HS Clock Delta UI (ΔUI)

This test verifies that the frequency stability of the DUT HS clock during a single burst is within the conformance limit.

Refer to *Test 1.4.17* to test the UI of the clock signal. ΔUI (UI variation) is a device's Unit Interval variation within a single HS burst. It is expressed in percentage.

Test Procedures

Refer to *Group4 Test Procedures* to perform the test.

NOTE



Requirements

This test requires you to configure the following parameters in *Analysis Settings*. Set the D-PHY Version to "V1.1" or "V1.2"; set the High-Speed Rate to ">1Gbps and ≤1.5 Gbps" or ">1.5Gbps and ≤2.5 Gbps".

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
ΔUI	≤1 Gbps	-10%	10%
	>1 Gbps and ≤ 1.5 Gbps	-5%	5%

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 10.1, Table 26.

12 Group 5 HS-TX Clock-to-Data Lane Timing Requirements

This section introduces the test methods for the test items of Group5 when you select "Normal" or "Normal+Escape" as the test mode in *System Settings*. If you select "Continuous Data" as the clock mode, refer to descriptions in *Continuous Data Test Mode*.

This group of tests verify various requirements regarding clock lane and data lane timing when the DUT is in HS mode.

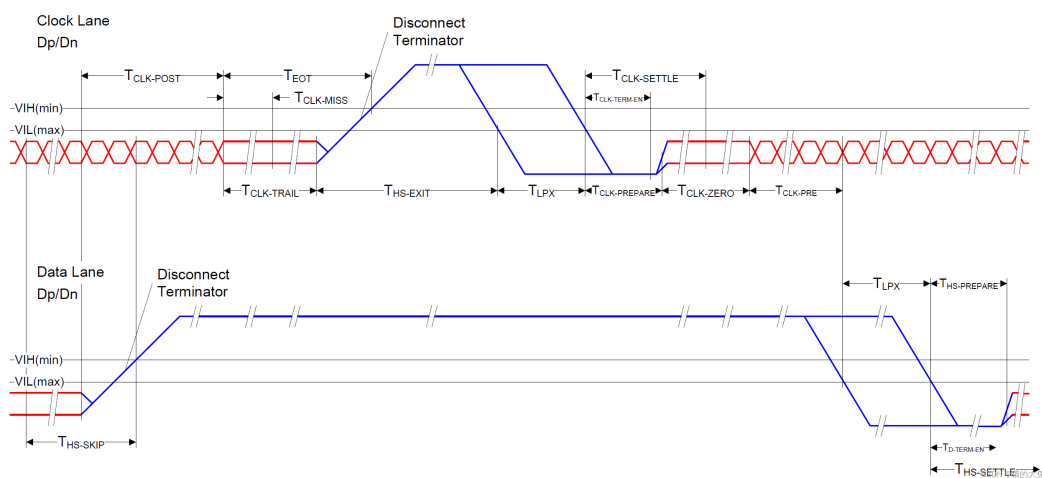


Figure 12.1 Switch the Clock Lane between Clock Transmission and Low-Power Mode

- Sequence when the clock lane enters the high-speed mode (HS Entry): LP11->LP10(T_{LPX})->LP00($T_{CLK-PREPARE}$)->HS0($T_{CLK-ZERO}$)-> $T_{CLK-PRE}$
- Sequence when the clock lane exits the high-speed mode (HS Exit): HS0/HS1-> $T_{CLK-POST}$ end with HS0-> $T_{CLK-TRAIL}$ ->LP-11($T_{HS-EXIT}$)

NOTE

This group of tests are generally performed on the master DUT, and they are not available for slave DUT.

12.1 Group 5 Test Procedures

Connect the oscilloscope, active probe, RTB test fixture, and DUT. For detailed connection methods, refer to *To Connect via the RTB Fixture* or *To Connect the Clock Lane and Data Lane*.

Open the MIPI compliance test interface, as shown in *Figure 6.1*.

Requirements

1. Click or tap the "System Settings" tab to configure the test.
 - Select the desired D-PHY version and High-Speed Rate according to the actual situation of the DUT.
 - Select "Escape" or "Normal+Escape" from the drop-down button of "Test Mode".
 - Click or tap the drop-down button of **Clock Mode** to select "Normal".
 - Based on the test device connection, select "CH1" as the D+ source and "CH3" as the D- source of the Data Lane. Select "CH2" as the D+ source and "CH4" as the D- source of the Clock Lane.

For the different configurations in the "System Settings" tab for the test items of Group5, refer to descriptions in *Table 6.7 Different Scenarios for Different Test Items of Group5*.

2. Click or tap the "Test Item" tab, and check the checkbox of Group5 and all of test items under it.
 3. Observe the specified waveform sequence captured by the oscilloscope on the clock lane.
 4. Click or tap the "Analysis Settings" tab. Click or tap **Start** to perform the test according to its instructions.
 5. Click or tap the "Result Export" tab to configure the result export, save and export the report.
- Analyze the test report, and observe the test results for each test item.
6. If the DUT has multiple data lanes, repeat the test procedures mentioned above to complete the test for all the data lanes.

12.2 Test 1.5.1 HS Entry: $T_{\text{CLK-PRE}}$ Value

This test verifies that the HS clock is driven prior to an associated data lane beginning the transition from LP to HS mode ($T_{\text{CLK-PRE}}$) is greater than the minimum required value.

Configure the DUT to send repeated HS burst sequences, as shown in *Figure 12.1*. Wherein, $T_{\text{CLK-PRE}}$ interval is measured from the end of the clock lane $T_{\text{CLK-ZERO}}$ interval (at the point where the clock lane differential waveform crosses below the minimum valid HS-RX differential threshold level of ± 70 mV) to the point where the data lane's V_{Dp} LP-01 falling edge crosses $V_{\text{IL,MAX}}$ (550 mV).

Test Procedures

Configure the DUT to send high-speed burst signal, as shown in [Figure 12.1](#).

Refer to [Group 5 Test Procedures](#) to perform the test.

NOTE

To perform the test, configure the parameters in [Analysis Settings](#). Set Clock Mode to "Normal"; set the Clock Lane Probing to "Differential".

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$T_{\text{CLK-PRE}}$	-	$(8 \times UI)$ ns	-

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.9, Table 14.

Test Result Reference



Figure 12.2 Test 1.5.1 Test Waveform and Result

12.3 Test 1.5.2 HS Exit: $T_{\text{CLK-POST}}$ Value

This test verifies that the DUT clock lane HS transmitter continues to transmit clock signaling for the minimum required duration ($T_{\text{CLK-POST}}$) after the last data lane switches to LP mode, as shown in [Figure 12.1](#).

$T_{\text{CLK-POST}}$ interval is measured from the end of the data lane $T_{\text{CLK-TRAIL}}$ period to the start of the clock lane $T_{\text{CLK-TRAIL}}$ period. For definitions for the $T_{\text{CLK-TRAIL}}$ and $T_{\text{CLK-TRAIL}}$ intervals, refer to [Test 1.3.13](#) and [Test 1.4.13](#).

Requirements

Test Procedures

Configure the DUT to send high-speed burst signal, as shown in [Figure 12.1](#).

Refer to [Group 5 Test Procedures](#) to perform the test.

NOTE

To perform the test, configure the parameters in [Analysis Settings](#). Set Clock Mode to "Normal"; set the Clock Lane Probing to "Differential".

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$T_{CLK-POST}$	-	(60 ns + 52*UI) ns	-

Wherein, UI is the nominal HS Unit Interval for the DUT, see [Test 1.4.17](#).

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.9, Table 14.

Test Result Reference



Figure 12.3 Test 1.5.2 Test Waveform and Result

12.4 Test 1.5.3 HS Clock Rising Edge Alignment to First Payload Bit

This test verifies whether the DUT HS clock is properly aligned to the payload data signaling.

Configure the DUT to send repeated data lane HS burst sequences. Use the oscilloscope to observe the clock and data lane signals in real-time manner, as shown

in [Figure 12.1](#). Verify that the first payload bit of burst data (i.e., the first bit after the Sync byte) aligns with a rising edge of the DDR clock, as shown in the figure below.

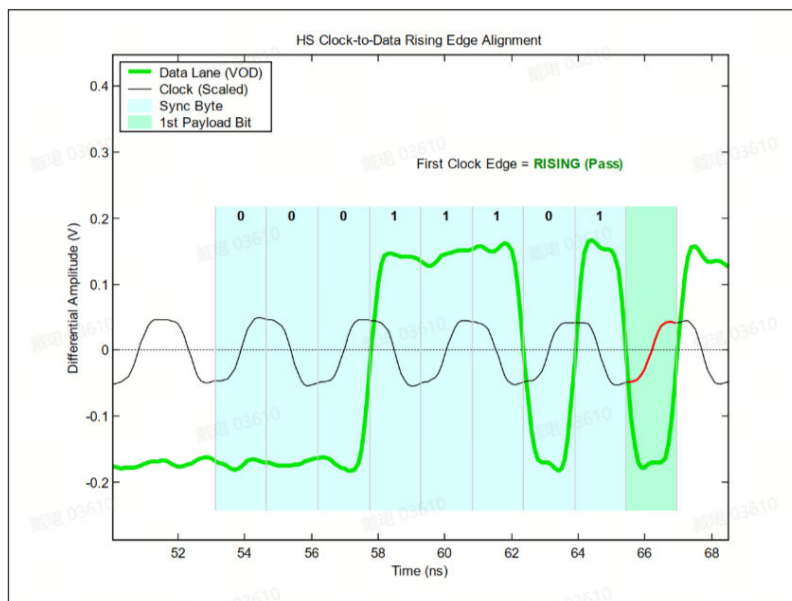


Figure 12.4 HS Clock-to-Data Rising Edge Alignment

Test Procedures

Configure the DUT to send high-speed burst signal, as shown in [Figure 12.1](#).

Refer to [Group 5 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Verify that the first payload bit of burst data aligns with a rising edge of the DDR clock.

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 10.2.

Test Result Reference

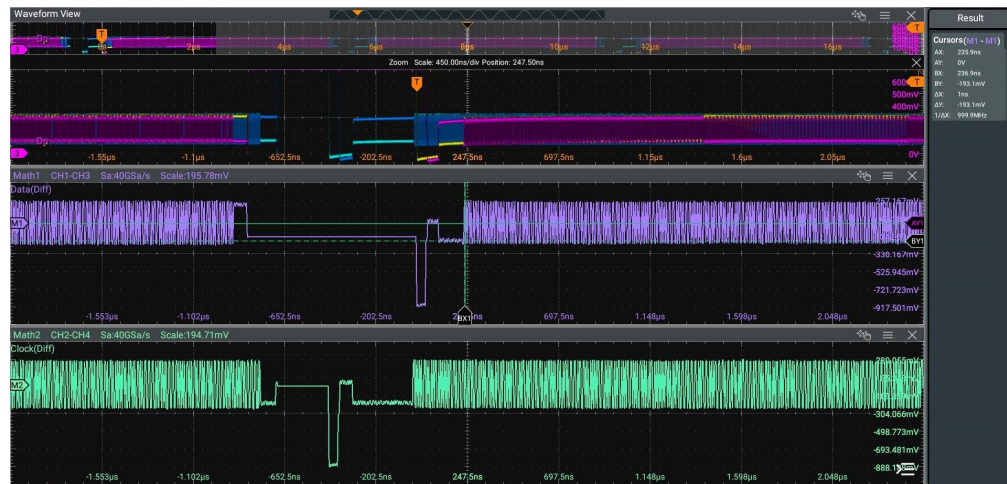


Figure 12.5 Test 1.5.3 Test Waveform and Result

12.5 Test 1.5.4 Data to Clock Skew ($T_{\text{SKEW}[\text{TX}]}$)

This test verifies that the skew between the clock and data signaling, as measured at the transmitter ($T_{\text{SKEW}[\text{TX}]}$) is within the conformance limit.

$T_{\text{SKEW}[\text{TX}]}$ is the allowed deviation of the data launch time to the ideal $\frac{1}{2}UI_{\text{INST}}$ displaced quadrature clock edge. As shown in the figure below, The timing error, $T_{\text{SKEW}[\text{TX}]}$, between each data lane edge and its respective clock lane edge will be computed over a minimum of 10,000 edges, to produce an array of timing error values. The maximum, minimum, and mean timing error values measured across all observed edges will be recorded.

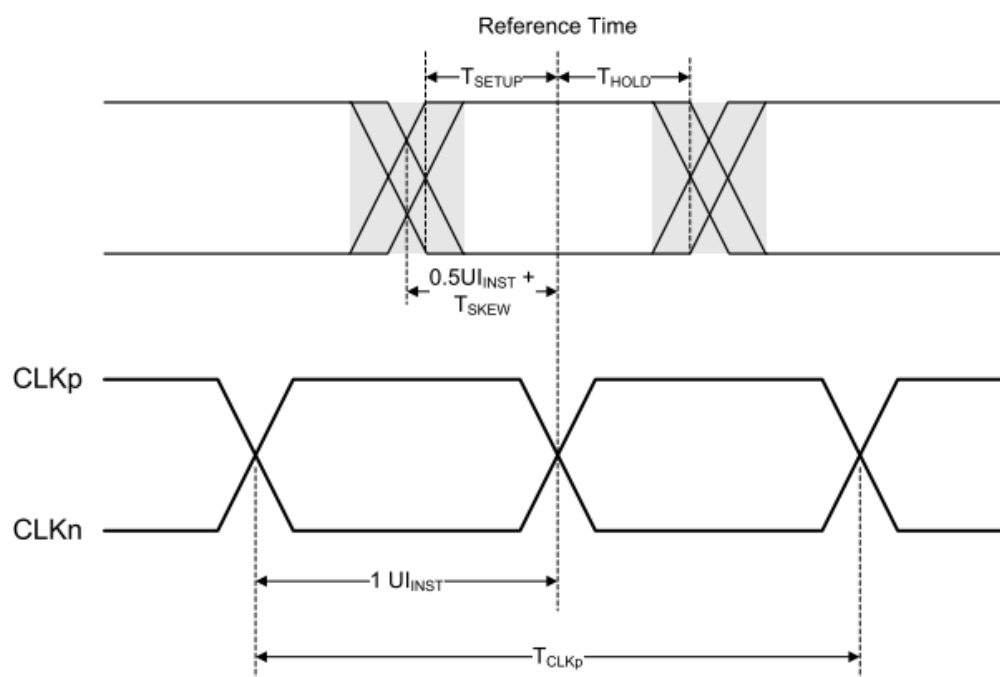


Figure 12.6 Data-to-Clock Timing Definitions

Test Procedures

Configure the DUT to send high-speed burst signal, as shown in [Figure 12.1](#).

Refer to [Group 5 Test Procedures](#) to perform the test.

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
$T_{\text{SKEW[TX]}}$	$\leq 1 \text{ Gbps}$	$(0.5 - 0.15) \cdot UI$	$(0.5 + 0.15) \cdot UI$
	$> 1 \text{ Gbps}$	$(0.5 - 0.2) \cdot UI$	$(0.5 + 0.2) \cdot UI$

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 10.2.1, Table 30.

Test Result Reference

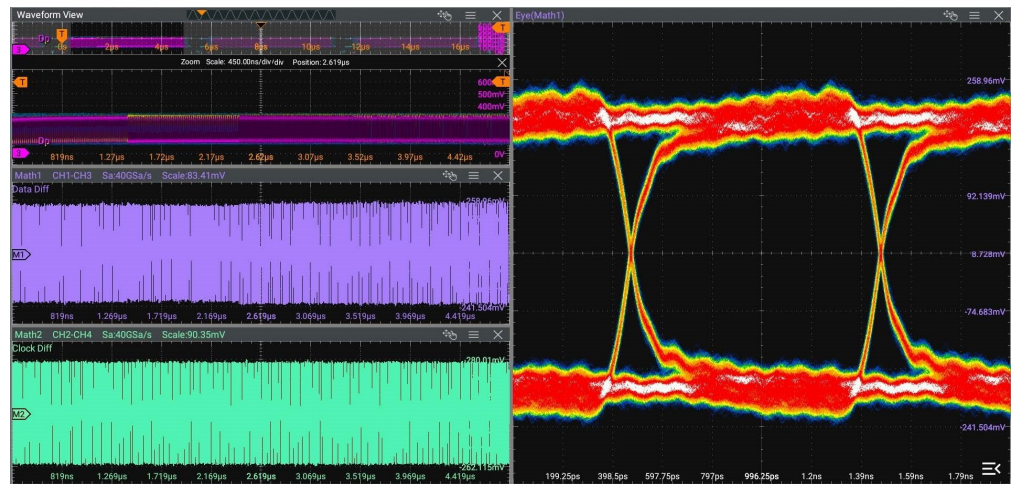


Figure 12.7 Test 1.5.4 Test Waveform and Result

12.6 Test 1.5.5 Initial HS Skew Calibration Burst ($T_{\text{SKEWCAL-SYNC}}$, T_{SKEWCAL})

This test verifies that the DUT transmits a validly formed initial HS skew calibration burst.

In this test, configure the DUT to send an initial HS skew calibration burst on the data lane, as shown in the figure below. For period deskew calibration, measure $T_{\text{SKEWCAL-SYNC}}$ and T_{SKEWCAL} interval values. This test item is only available for the DUT operating above 1.5 Gbps.

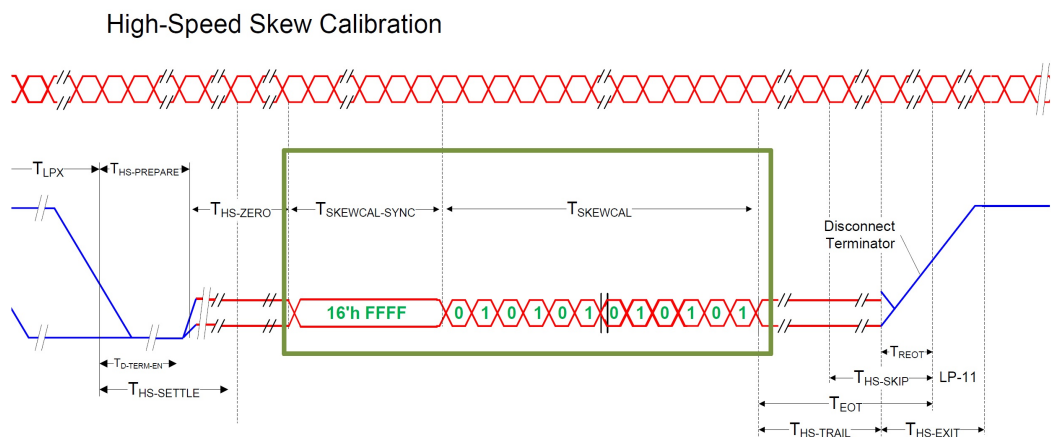


Figure 12.8 High-Speed Skew Calibration Burst

Test Procedures

Configure the DUT to send high-speed burst signal, as shown in [Figure 12.8](#).

Refer to *Group 5 Test Procedures* to perform the test.



NOTE

This test requires you to configure the following parameters in *Analysis Settings*. Set the D-PHY Version to "V1.2"; set the High-Speed Rate to ">1.5Gbps and ≤2.5 Gbps".

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
T _{SKEWCAL-SYNC}	> 1.5 Gbps	(16 - 0.25)*UI	(16 + 0.25)*UI
T _{SKEWCAL}		2 ¹⁵ *UI (32768*UI)	

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.12.

12.7 Test 1.5.6 Periodic HS Skew Calibration Burst (T_{SKEWCAL-SYNC}, T_{SKEWCAL})

This test verifies that the DUT transmits a validly formed periodic HS skew calibration burst.

Refer to *Test 1.5.5* to measure T_{SKEWCAL-SYNC} and T_{SKEWCAL} interval values. The specification, requirement, and procedures of this test are similar with those of Test 1.5.5, except the periodic deskew burst is measured instead of the initial burst.

Test Procedures

Configure the DUT to send high-speed burst signal, as shown in *Figure 12.8*.

Refer to *Group 5 Test Procedures* to perform the test.



NOTE

This test requires you to configure the following parameters in *Analysis Settings*. Set the D-PHY Version to "V1.2"; set the High-Speed Rate to ">1.5Gbps and ≤2.5 Gbps".

Pass Conditions

The test results shall meet the following conditions:

Parameter	DUT Rate	Min.	Max.
T _{SKEWCAL-SYNC}	> 1.5 Gbps	(16 - 0.25)*UI	(16 + 0.25)*UI
T _{SKEWCAL}		2 ¹² *UI (4096*UI)	

Requirements

Reference Protocol

Refer to D-PHY Specification (v1.2), Section 6.12.

13 Eye Diagram Test

This section introduces the test methods for the Eye Diagram Test when you select "Normal" or "Normal+Escape" as the test mode in *System Settings*. If you select "Continuous Data" as the clock mode, refer to descriptions in *Continuous Data Test Mode*.

This test item is the standard test item not specified in the Specification. It is only used to measure and capture the data signal sent from the DUT in high-speed mode, obtain the generated eye diagram and measure its eye width and eye height. For the DS70000 and DS80000 series oscilloscope, to perform this test, the eye diagram option is required to be installed.

Connect the Device

Connect the oscilloscope, active probe, RTB test fixture, and DUT. The connection methods are the same as those for test items of Group3, Group4, and Group 5. For detailed connection methods, refer to *To Connect via the RTB Fixture* or *To Connect the Clock Lane and Data Lane*.

Configure the DUT

Refer to configurations in Group3, Group4, or Group5, configure the data lane of the DUT to enter the high-speed burst data transmission state to send the high-speed data burst sequence.

Configure the oscilloscope to perform the MIPI compliance test

Open the MIPI compliance test interface, as shown in *Figure 6.1*.

1. Click or tap the "System Settings" tab to configure the test.
 - Select the desired D-PHY version and High-Speed Rate according to the actual situation of the DUT.
 - Select "Escape" or "Normal+Escape" from the drop-down button of "Test Mode".
 - Based on the test device connection, select "CH1" as the D+ source and "CH3" as the D- source of the Data Lane. Select "CH2" as the D+ source and "CH4" as the D- source of the Clock Lane.
2. In the "Test Item" tab, check the checkbox of Eye Diagram and its two sub-items (HS Data Eye Height and HS Data Eye Width).
3. Observe the specified waveform sequence captured by the oscilloscope on the clock lane.

4. Click or tap the "Analysis Settings" tab. Click or tap **Start** to perform the test according to its instructions.
5. Click or tap the "Result Export" tab to configure the result export, save and export the report.

Make an analysis on the test report and view the eye height and eye width of the generated eye diagram.

6. If the DUT has multiple data lanes, repeat the test procedures mentioned above to complete the test for all the data lanes.

14 Continuous Data Test Mode

This section introduces the test methods for Continuous Data mode selected in *System Settings*.

Continuous Data mode is the standard working mode not specified in MIPI PHY Specification. It is only available for the specified test items when the data lane and clock lane of the DUT output continuous high-speed signal. For the detailed test items supported, refer to *Test Items for Continuous Data Test*.

Connect the Device

Connect the oscilloscope to the DUT. For detailed connection methods, refer to *Continuous Data Test Connection*.

Configure the DUT

Configure the DUT to send continuous high-speed data signal and clock signal.

Configure the oscilloscope to perform the MIPI compliance test

Open the MIPI compliance test interface, as shown in *Figure 6.1*.

1. Click or tap the "System Settings" tab to configure the test.
 - Select the desired D-PHY version and High-Speed Rate according to the actual situation of the DUT.
 - Click or tap the drop-down button of **Test Mode** to select "Continuous Data".
 - Click or tap the drop-down button of **Clock Mode** to select "Continuous".
 - Based on the test device connection, select "CH1" as the D+ source and "CH3" as the D- source of the Data Lane. Select "CH2" as the D+ source and "CH4" as the D- source of the Clock Lane.
2. Click or tap the "Test Item" tab, and check the checkbox of Group3 and all of test items under it.
3. Observe the HS continuous waveform sequence captured by the oscilloscope on the clock lane and data lane.
4. Click or tap the "Analysis Settings" tab. Click or tap **Start** to perform the test according to its instructions.
5. Click or tap the "Result Export" tab to configure the result export, save and export the report.

Analyze the test report, and observe the test results for each test item.

6. If the DUT has multiple data lanes, repeat the test procedures mentioned above to complete the test for all the data lanes.

15 Appendix

15.1 Appendix B: Warranty

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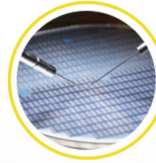
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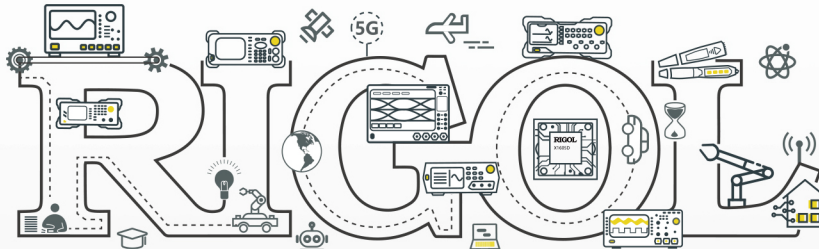
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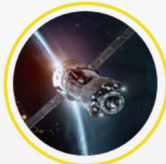


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